5. Final remarks

There are two aspects concerning the multichannel ASIC design. The one is electronic point of view on new solutions, quality of design and on taking the advantages offered by VLSI technology. The other refers to a more practical side, when the ASICs are used in real multichannel systems, and then the question arises about the new possibilities in given experimental technique thanks to the use of our ASICs.

From the electronic point of view the important aspects which have been solved for the presented chips are as follows:

– **for RX64 IC:**
  - low level of noise, together with the low power consumption and high counting rate performance which makes it possible to perform the measurements at a room temperature using RX64 for low input amplitude signals appearing at the input with high frequency;
  - very good matching performance from channel-to-channel which is essential for the quality of the multichannel system;
  - implementation in chip digital blocks for data storage, control, communication and testing which increases the functionality, testability and reliability of IC;
  - minimisation in mixed-mode chip effects of crosstalk to the negligible level;
  - small area of the chip and relatively low cost;

– **for NEURO64:**
  - low noise level due to proper 1/f noise optimisation;
  - new AC coupling of small area with a cut-off frequency at the order of mHz;
  - new concept of continuous-time filters;
  - minimised spread of main analogue parameters, as gain and cut-off frequencies, from channel-to-channel;
  - small area and small power consumption.

Both chips have found practical applications in scientific research carried out in physics and biology. They open new possibilities in experimental techniques. The RX64 chips together with the silicon strip detector have been installed at the powder diffractometer with the Bragg-Bretano focusing used for polycrystal and thin film structures investigations. The obtained spatial resolution is comparable with the resolution offered by the conventional detection system, while the measurement time is reduced by two orders of magnitude. This is a new quality in diffraction experimental techniques making for example, observation of dynamic processes like phase transitions possible. The NEURO64 chips are used in the

Retinal Readout System to understand the processing and encoding of visual information in the eye. All commercially offered multichannel readout systems for these purposes do not exceed one hundred channels. The NEURO64 chips due to low noise performance, low power consumption and uniformity of analogue parameters from channel-to channel are dedicated to build in the near future a readout system for imaging the neural activity of retinal output neurones on a scale one order of magnitude greater than the existing so far.

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Appendix I

Let us consider a folded cascode amplifier shown in Figure A.1a. An equivalent small signal circuit of the amplifier for the low frequency range is shown in Figure A.1b.

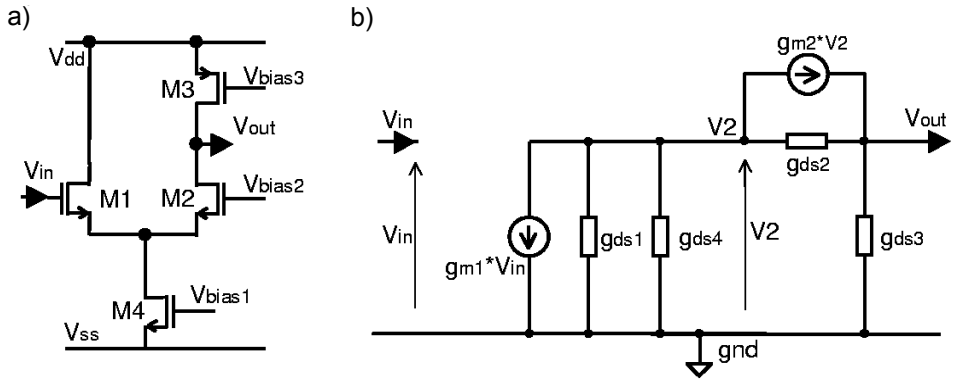

Fig. A.1. Folded cascode amplifier: a) scheme; b) equivalent small signal circuit

Applying a voltage signal source v_{in} at the input and summing currents at nodes v_2 and v_{out} in circuit from Figure A.1b, we have

$$-g_{m1}v_{in} - v_2(g_{ds1} + g_{ds4}) + (v_{out} - v_2)g_{ds2} - g_{m2}v_2 = 0 \tag{A.1}$$

$$(v_{out} - v_2)g_{ds2} + v_{out}g_{ds3} - g_{m2}v_2 = 0 \tag{A.2}$$

Solving the above equations one obtains

$$\frac{v_{out}}{v_{in}} = -\frac{g_{m1}(g_{m2} + g_{ds2})}{g_{ds2}(g_{ds1} + g_{ds4}) + g_{ds3}(g_{m2} + g_{ds1} + g_{ds2} + g_{ds4})} \tag{A.3}$$

Keeping in mind that in this particular project $g_{m2} >> g_{ds1}$, g_{ds2}, g_{ds4} and $g_{ds3} \approx g_{ds2}$ we obtain

$$\frac{v_{out}}{v_{in}} \approx -\frac{g_{m1}}{g_{ds3}} \tag{A.4}$$

The equivalent small signal model of the folded cascode amplifier can be simplified as shown in Figure A.2.

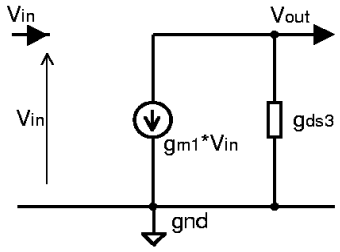

Fig. A.2. Simplified small signal equivalent circuit of the folded cascode amplifier for the low frequency range

Taking formulae for g_{m1} and g_{ds3} equation (A.4) can be rewritten as

$$\frac{v_{out}}{v_{in}} \approx -\frac{\sqrt{2\mu_p C_{ox} \frac{W_1}{L_1} I_{DS1}}}{\lambda_3 I_{DS3}} \tag{A.5}$$

Appendix II

Let us consider a simplified small signal diagram of the folded cascode amplifier with two elements C_1 and g_{ds5} in the feedback loop, as it is shown in Figure A.3.

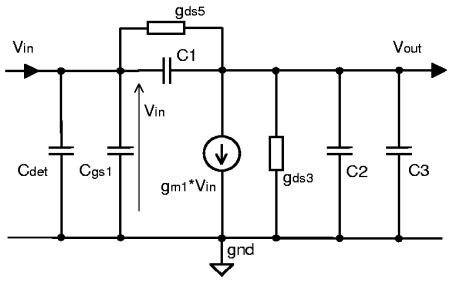

Fig. A.3. Simplified small signal model of the preamplifier from Figure 3.7

Let us connect two additional capacitors C_{det} and C_{gs1} at the input and two capacitors C_2 and C_3 at the output. According to the scheme of the preamplifier shown in Figure 3.7 C_{gs1} corresponds to gate-source capacitance of transistor M1, g_{ds5} is a source-drain conductance of transistor M5, while C_1, C_2 and C_3 are capacitors in the feedback and at the output of the preamplifier. The capacitor C_{det} in Figure A.3 represents the total capacitance of detector connected to the input of the preamplifier.

Applying a current δ-like pulse of the amplitude i_{in} at the input of the circuit in Figure A.3 and summing currents at nodes v_{in} and v_{out} , we have

$$i_{in} - v_{in}(sC_{det} + sC_{gs1}) - (v_{in} - v_{out})(g_{ds5} + sC_1) = 0 \tag{A.6}$$

$$(v_{in} - v_{out})(g_{ds5} + sC_1) - g_{m1}v_{in} - v_{out}(g_{ds3} + sC_2 + sC_3) = 0 \tag{A.7}$$

Solving above equations one obtains

$$\frac{v_{out}}{i_{in}} = \frac{sC_1 - g_{m1} + g_{ds5}}{as^2 + bs + c} \tag{A.8}$$

where a, b and c are equal

$$a = (C_2 + C_3)(C_{det} + C_{gs1}) + C_1(C_{det} + C_{gs1}) + C_1(C_2 + C_3) \tag{A.9}$$

$$b = g_{m1}C_1 + (g_{ds3} + g_{ds5})(C_{det} + C_{gs1}) + g_{ds5}(C_2 + C_3) + g_{ds3}C_1 \tag{A.10}$$

$$c = g_{ds5}(g_{m1} + g_{ds3}) \tag{A.11}$$

Dropping less significant terms in the above equations one can rewrite equation (A.8) as

$$\frac{v_{out}}{i_{in}} \approx \frac{sC_1 - g_{m1}}{s^2(C_2 + C_3)(C_{det} + C_{gs1}) + sg_{m1}C_1 + g_{m1}g_{ds5}} \tag{A.12}$$

The above transfer function has one zero at high frequency $z = g_{m1}/C_1$ and two poles, which are widely separated in frequency $|p_1| << |p_2|$ and can be expressed as

$$p_1 \approx -\frac{g_{ds5}}{C_1} \tag{A.13}$$

$$p_2 \approx -\frac{g_{m1}C_1}{(C_2 + C_3)(C_{det} + C_{gs1})} \tag{A.14}$$

Appendix III

Let us consider the shaper amplifier in Figure 3.8. An equivalent small signal diagram of this circuits is shown in Figure A.4. According to the scheme of the shaper (Fig. 3.8) C_{gs14} corresponds to gate-source capacitance of transistor M14, g_{m14} is a gate transconductance of transistor M14, g_{ds16} and g_{ds18} are source-drain conductances of transistors M16 and M18, C_{os} is total capacitance to the ground seen from the drain of transistor M16, while C_4 and C_5 are the same capacitors as shown in Figure 3.8.

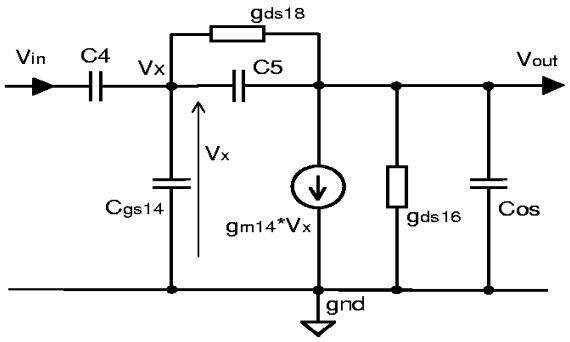

Fig. A.4. Simplified small signal model of the shaper from Figure 3.8

Applying a voltage signal at node v_{in} and summing currents at nodes v_x and v_{out}, one can write following equations

$$(v_{in} - v_x)sC_4 - v_x sC_{gs14} - (v_x - v_{out})(g_{ds18} + sC_4) = 0 \tag{A.15}$$

$$(v_x - v_{out})(g_{ds18} + sC_4) - g_{m14}v_x - v_{out}(g_{ds16} + sC_{os}) = 0 \tag{A.16}$$

Solving above equations one can find the frequency response of the shaper.

Since in our case C_4 is much bigger than C_{gs14}, C_{os}, C_5 and g_{m14} is much bigger than g_{ds16}, gds_{18} , neglecting less significant term one can write the frequency response of the shaper as

$$\frac{v_{out}}{v_{in}} \approx \frac{sC_4\left(sC_5 - g_{m14}\right)}{s^2C_4\left(C_{os} + C_5\right) + sg_{m14}C_5 + g_{m14}g_{ds18}} \tag{A.17}$$

This response has two zeros z_1 and z_2

$$\begin{aligned} z_1 &= 0 \\ z_2 &= \frac{g_{m14}}{C_5} \end{aligned} \tag{A.18}$$

with z_2 being negligible as located in the very high frequency region. Since in our case $|p_1| << |p_2|$, the dominant pole p_1 and the second one p_2 can be written as

$$\begin{aligned} p_1 &\approx -\frac{g_{ds18}}{C_5} \\ p_2 &\approx -\frac{g_{m14}C_5}{C_4\left(C_{os} + C_5\right)} \end{aligned} \tag{A.19}$$

Appendix IV

Let us consider a simplified circuit diagram of the core part of NEURO64 filter shown in Figure A.5.

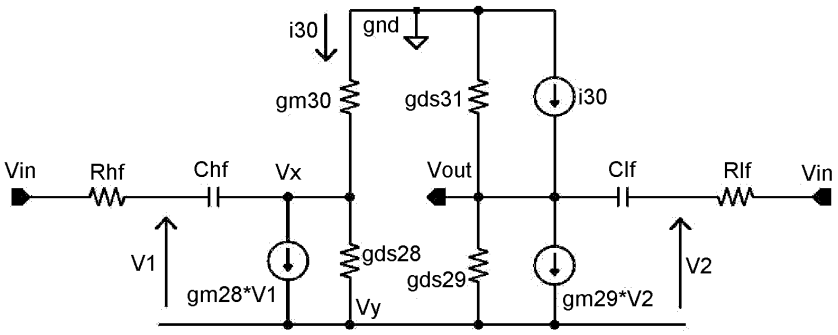

Fig. A.5. Simplified small signal circuit of the band-pass filter

Applying a voltage signal at node v_{in} and summing currents at nodes v_x, v_{out} and v_y, one can write following equations

$$(v_{in} - v_x)G_{hf} + (v_y - v_x)g_{ds28} - v_x g_{m30} - g_{m28}v_1 = 0 \tag{A.20}$$

$$(v_{in} - v_{out})G_{lf} + (v_y - v_{out})g_{ds29} - v_{out}g_{ds31} - v_x g_{m30} - g_{m29}v_2 = 0 \tag{A.21}$$

$$g_{m28}v_1 + g_{m29}v_2 - (v_y - v_x)g_{ds28} + (v_y - v_{out})g_{ds29} = 0 \tag{A.22}$$

where $G_{hf}=1/(R_{hf}+1/sC_{hf})$ and $G_{lf}=1/(R_{lf}+1/sC_{lf})$.

Voltages v_1 and v_2 can be expressed as

$$v_1 = v_x - v_y + (v_{in} - v_x) G_{hf} \frac{1}{sC_{hf}} \tag{A.23}$$

$$v_2 = v_{out} - v_y + (v_{in} - v_{out}) G_{lf} \frac{1}{sC_{lf}} \tag{A.24}$$

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