4. Low noise multichannel IC for recording neuronal signals using microelectrode array

In this chapter we present another example of multichannel ASIC for readout of neuronal signals from neuronal network. The nature of neuronal signals is very different compared to the signals from silicon strip detectors, however, they are also small and have to be recorded simultaneously from many electrodes. Thus low noise and matching are absolutely critical design aspects in multichannel ASICs for readout such signals.

A neuron, or nerve cell, is the basic unit processing information in the human organism. Early in this century scientists realised that neurones could process information by generating electric pulses called action potentials. For many years, neuroscientists have recorded signals only from one neuronal cell at a time. Much is known about neuronal cell structure and the operation and physiology of single cell. But neurones are organised in large systems and next to nothing is known about the organisational principles of the collective behaviour of neuronal networks. To understand the mechanisms of information processing in the correlated activity of different cells simultaneous detection of signals from many neuronal cells is necessary [3, 5, 90]. One of such neuronal systems which has been studied extensively by neurobiologists for many years is the vertebrate retina.

The vertebrate retina is a layer neuronal network, about 200 μm thick, that lines the back of the eye. It converts the visual image generated by the eye's optics into a pattern of neural activity, processes this signal, extracting from it certain features of interest to the organism, and transmits the result of these computations in the form of electric spikes to the brain. The retina offers many advantages for the study of neural processing. It can be readily isolated from the eye without the damage to internal connections, and maintains its functions *in vitro* over many hours [91]. Furthermore, the circuit has a clearly defined and easily controlled input, namely the visual image focused on the photoreceptors. It also generates a clearly defined output, namely action potentials in the retinal ganglion cells. By placing an isolated retina on a flat micloelectrode array, one can record simultaneously extracellular action potentials from many retinal ganglion cells.

For the instrumentation of such an experiment, one needs a high density multielectrode array and a multichannel readout electronic system. Such a multichannel readout electronic system based on the ASIC called NEURO64 is the subject of this chapter. The main aim of this integrated circuit is to amplify and filter small retinal signals collected by a planar multielectrode array [5]. To understand better the requirements for the ASIC, we firstly describe the nature of neuronal signals and the geometry of multielectrode planar array dedicated to the extracellular recording. We also briefly review some existing solutions of the readout systems and formulate the requirements for the readout electronics which are

specific for the experiments with live retina. Subsequently, the architecture of multichannel NEURO64 chip dedicated to the above experiments is described. We analyse successive stages of the IC design and present the measured electrical parameters of the circuit. At the end, some exemplary results obtained from an experiment using the NEURO64 chip in neurobiological measurements with vertebrate retina are briefly discussed.

4.1. Extracellular recording

Neuronal signals can be measured using intracellular or extracellular recording. An intracellular signal is known as a membrane potential, since the voltage signal is due to the electrical imbalance (among Na, K and Cl ions) across the biological membrane. Conversely, an extracellular signal arises from the electrical charge imbalance near the outside of the biological membrane. In contrast to the intracellular potential, this potential is recorded outside the neuronal membrane with respect to the neutral extracellular fluid as diagrammed in Figure 4.1. Moreover, the extracellular potential is typically in the microvolt range, while the intracellular potential is measured in milivolts [92].

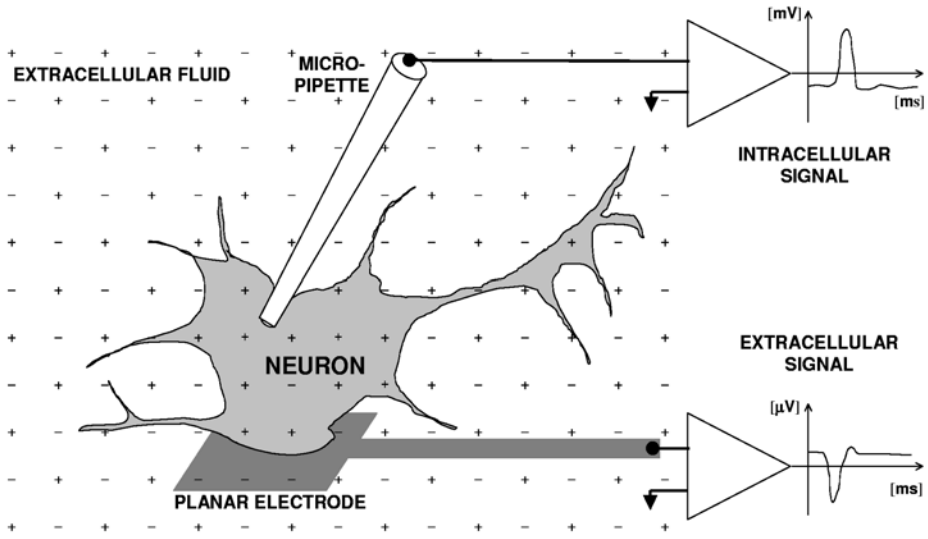

Fig. 4.1. Typical intracellular and extracellular neuron recording techniques

4.1.1. Multielectrode array

To obtain a more complete picture of the neuronal network behaviour, one needs an experimental method to record simultaneously neuronal activity from many neurones. One of the most popular techniques for studying the operation principles of neuronal systems is based on using a planar multielectrode array for extracellular recording. There is a wide variety of mulielectrode arrays depending on the type of neuronal activity to be studied

[90, 93, 94]. A typical probe for studying brain slices is an array of 64 planar microelectrodes, each having a size 50 × 50 μm^2 arranged in 8 by 8 patterns with 150 μm separation [90]. This probe can be used both for the electrical stimulation of the neurones and for recording the extracellular signal. The experiment carried out to investigate spontaneous activity in cortical slices [93] also uses 64 recording electrodes, each of 30 × 30 μm^2.

Microelectrode arrays for studying the retinal tissue must have smaller dimensions, because of the smaller sizes of ganglion cells. An example of the 61 electrode array geometry used in Retinal Readout System [95] is shown in Figure 4.2. The electrode spacing is 60 μm and the electrode dimensions are 15 × 15 μm^2 or in some cases 5 × 5 μm^2. The retina tissue requires optical stimulation and the recording of electrical signals. Therefore the multielectrode array must be transparent to transmit light. This electrode array is produced on a transparent glass substrate with indium tin oxide (about 150 nm thick). Silicon nitride, 2 μm thick, forms an insulating layer. Openings in this layer are left for electrodes and wire bonding pads. The electrodes are platinized to reduce the impedance of interface with the saline solution. The wire bond pads are formed from 1 μm thick aluminium.

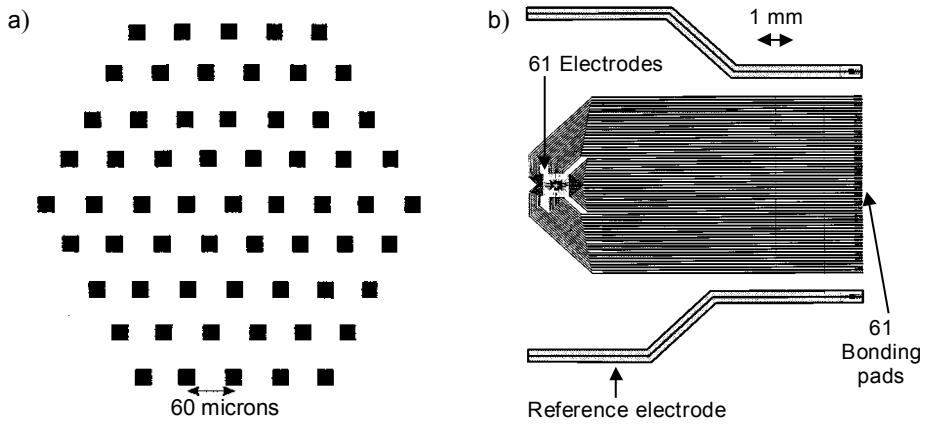

Fig 4.2. The multielectrode array for the Retinal Readout System: a) the electrode geometry – each black square represents a platinized electrode with dimensions 15 μm × 15 μm; b) complete layout of 61 electrode array

One should realise that even 61 electrodes in a retina experiment with a typical electrode spacing cover only an area of 0.17 mm^2, while the total area of the human retina is about 10 cm^2. Nowadays there are two limiting factors for the number of electrodes within one array, namely the technology used for array manufacturing and the readout electronics. The technologies of microelectrode arrays are based on custom developed processes involving the technology of ITO (indium tin oxide), and they are essentially equivalent to the silicon processes with a single metal layer. This imposes serious limitation on the layout of tracks connecting the electrodes to the fanout which enables the connections of the readout electronics. Pushing this technology to the limit 519 electrode array dedicated to the retina study has been designed [94]. The electrode spacing is 60 μm, with the electrode size between 2 and 5 μm. The track width for this design is 2 μm, which allows all the 519 tracks

to be taken out to the edge where they are connected to bond pads. In order to use such an electrode array effectively, one needs an appropriate readout system, which basically has to comprise as many independent electronic channels as the number of electrodes.

4.1.2. Readout electronics for extracellular recording

Recording extracellular signals is practically a non-invasive method but the signals at the electrodes are small. The recorded signals have the form of separated spikes of amplitudes from tens to hundreds of microvolts and the duration time of the order of miliseconds. Therefore, high performance low noise electronics is required to record and process such signals. Additionally, the extracellular signal has a DC offset which may significantly vary from electrode to electrode inside one multielectrode array. Therefore the first stage of readout electronics should tolerate these offsets or be AC coupled to the electrodes.

Multichannel readout systems for neurobiology applications are built mostly in hybrid technologies using components of the shelf. Typically each readout channel comprises a low noise preamplifier and a band pass filter. Since low noise is required the preamplifiers are usually built of discrete components using preferably JFETs as input devices and the AC coupling at the input. Multichannel readout systems are offered commercially up to 128-channel readout modules. Further increase of the number of channels becomes very unpractical because of the large volume occupied by the electronics which is connected to microelectrode arrays, and because of high cost. An obvious solution to overcome these problems is to employ the ASIC technique and develop ICs suitable for these purposes.

In the references pertaining to the subject there are a few examples of ASICs dedicated to extracellular recording [96, 97, 98, 99]. A multichannel recording probe design for long term monitoring of the neural activity in the central nervous systems is presented in [96]. This active probe supports 32 recording electrodes and selects eight signals at the input for further processing. The neural signals in the selected channels are then amplified and multiplexed to the external recording system. The amplifiers have a gain of about 350 V/V and the 3 dB bandwidth is from 15 Hz to 7 kHz. The input referred noise is 15 μV rms. To solve the problems of the input offsets the amplifier has a low frequency feedback to reduce the amplification of DC signals. The measured DC gain is near unity over the range from −50 mV to +150 mV at the input. The chip dissipates only 2.5 mW of power. The next generation of neural probe [97] has 64 electrodes both for stimulation and recording.

Another ASIC dedicated for the measurement of activity from electrically excitable cell from cardiac and neuronal tissues is presented in [98]. An amplifier/stimulator chip is implemented in the 2 μm CMOS technology. The ASIC includes 16 amplifiers with differential inputs and has possibility to send stimulation signals. The input referred noise over the 50 kHz bandwidth is 12−16 μV rms. Each amplifier has AC coupling at the input which is obtained by using a 10 nF discrete serial capacitor. This capacitor together with a 22 MΩ parallel resistor connected to the ground forms a high pass filter with corner frequency at 0.7 Hz. The total power consumption is 105 mW per chip.

An interesting ASIC for digital neural recording is described in [99]. The chip is designed for obtaining recordings of ±500 μV neural signals from axons regenerated through sieve electrodes. Every time 2 of 32 electrodes can be selected at the input for the following recording. The neuronal signals are amplified using 100 Hz to 3.1 kHz band limited amplifiers, multiplexed, and digitised with low power (below 2 mW), moderate speed (8 μs/b)

8-bit ADC. The chip is implemented in the 3 μm CMOS technology and dissipates 90 mW of power. Since the total system is powered and controlled employing an RF telemetry link, it can be used as an implant in an animal organism for the chronic neuronal recording application.

Each of the above mentioned ASICs has some extra features specific for a given application. Since we consider measurements of retina tissue, let us analyse the requirements for the readout electronics dedicated to this application.

4.1.3. Requirements for readout electronics dedicated to retina measurements

The main aim of neurobiological measurements employing vertebrate retina is to study how the retina processes, encodes and transmits information about the visual world to the brain. During the experiments the live retina tissue is placed on the planar multielectrode array inside a cylindrical chamber containing a physiological solution. A visual image is focused onto the retina, which converts the image into a set of electrical signals that in a live organism is sent via an optic nerve to the brain.

The cross-sectional view of the retina tissue is shown in Figure 4.3. Human retina consists of three main layers: the first one is formed by 10^8 photoreceptors (cones and rods), the second is an intermediate layer (horizontal, bipolar and amacrine cells) and the third one is built of ganglion cells whose axons form the optic nerve.

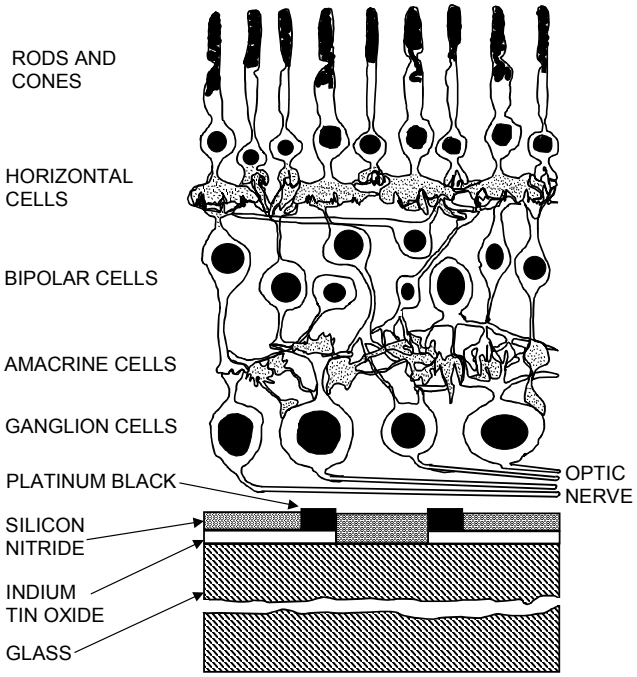

Fig. 4.3. Cross-sectional view of retinal tissue placed on top of multielectrode array

The photoreceptors in response to the absorbed photons generate the electrical signals. These signals are picked up by the intermediate retinal layer which performs sophisticated parallel analogue processing, followed by the output signal generation in the ganglion cell layer. From the ganglion cells the encoded information, in the form of voltage spikes, is sent to the brain via 10^6 optic nerve fibres. In our experiment these voltage spikes are collected by the multielectrode array and are further processed by the readout electronics.

The design of the NEURO64 IC is based on the earlier 32-channel prototype called NEURO32 which analogue parameters have been proved to be satisfactory for experiments with retina [100, 101]. The current project assumes a design of 64-channel ASICs dedicated to these measurements. At the first stage the IC should replace an old 61-channel recording system, built of discrete components, while in the other stage eight 64-channel ASICs will be used to build 512-electrode readout system.

The basic requirements concerning the features and the parameters of the new ASIC are as follows:

- multichannel architecture, which results in particular requirements with respect to the layout of ICs and the matching of analogue parameters from channel-to-channel;
- low noise performance because amplitudes of neural signals are typically in the range from 50 μV to 500 μV with the frequency spectrum which is in the range from 20 Hz to 2000 Hz [91]; a low noise preamplifier and a low frequency band-pass filter are required;
- large tolerance of the preamplifier towards the input offsets due to the fact that small neuronal signals are superimposed on much larger DC offsets;
- differential input, since the signals from the readout electrodes are measured with respect to a common reference electrode immersed in physiological saline solution;
- low power consumption per single channel (below 2 mW) to avoid the using of cooling system;
- possibility of controlling the gain of the preamplifier and corner frequencies of the filter;
- reduction of data output connections by using an analogue multiplexer.

4.2. Architecture of NEURO64 IC

A low signal amplitude and a low frequency spectrum of extracellular neuronal signals are a challenge to this design. A low noise preamplifier and proper shaping of the frequency band are required to optimise the signal to noise ratio. In most low frequency applications high precision switched-capacitor filters and digital ones play dominant role. Their non-negligible disadvantages are connected with the clock feed-through and with the fact that they produce more noise than their continuous-time RC counterparts [102]. Since the ultimate aim of our project is a system comprising several hundreds of electrodes, and respectively the same number of channels of the readout electronics, the area occupied by the filters and the power consumption of the readout electronics are important factors to be taken into account. The multichannel ASIC presented here employs continuous-time RC filter approach.

Figure 4.4 shows the block diagram of the developed IC called NEURO64. A single chip is designed to provide a readout of signals from 64 electrodes. It comprises three basic blocks: 64+5 channels of low-noise preamplifiers and two-stage band-pass filters, an analogue multiplexer 64:1, and a control circuit. Five additional analogue channels are added for the twofold purpose. Firstly, four most outer channels on each side of the chip play the role of dummy and test channels to guarantee good matching of analogue parameters for the 65 channels. Out of these 65 channels, 64 are used for recording signals from the electrodes and one channel is used as a dummy reference channel for the multiplexer. Secondly, those dummy channels are equipped with test pads which are used for the detailed evaluation of the basic analogue parameters such as noise, gain and filter frequency response. The power supplies and reference currents, which allow one to control the gain and frequency characteristics of the analogue part, are kept common for all 69 channels. The signals from the 64 channels are sampled at the same moment and subsequently multiplexed through the analogue multiplexer 64:1 to the output buffer.

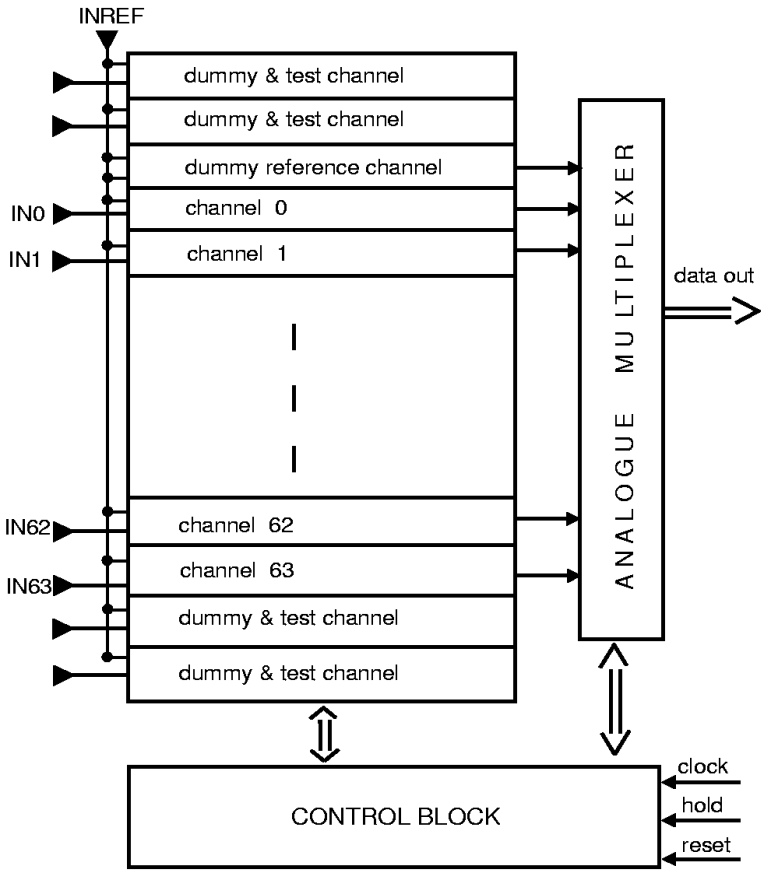

Fig. 4.4. Block diagram of NEURO64 chip

The required multiplexing rate in the developed retina readout system is up to 5 MHz, which is not very demanding from the point of view of the multiplexer design. Therefore, rather standard solutions are employed in the multiplexer scheme. In order to reduce possible common mode interference which may occur in a multichannel system, a dummy reference channel is implemented, which provides a reference signal for the differential output stage of the multiplexer. The IC has been manufactured in the MIETEC 0.7 μm CMOS process, which is known to have flicker noise lower when compared to other CMOS technologies.

4.3. Analogue signal processing chain

The block diagram of a single channel of the NEURO64 chip is shown in Figure 4.5. It comprises a preamplifier, two identical filter stages and an output amplifier. The signals from the readout electrodes are measured with respect to a reference electrode and therefore the input stage of the readout electronics has to be a differential one, although this solution increases the noise contribution from the input transistor by a factor √2 compared to a single ended configuration. In addition to the common mode input signals, one has to take into account significant differential offsets on the electrodes. Considering the range of the input signals from 50 μV to 500 μV the total gain of the order of 1000 V/V is needed to match a typical ADC range at the output. In order to avoid propagation of the offsets through the entire signal path the consecutive stages are AC coupled.

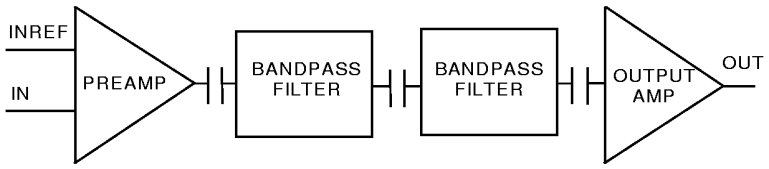

Fig. 4.5. Block diagram of the single front-end channel

4.3.1. Low noise preamplifier design

The amplifier design is optimised to meet first of all the requirements of low noise performance and tolerance to large input voltage offsets. From the standpoint of view of setting the amplifier gain those two requirements are contradictory. For the optimisation of noise a high gain in the first stage is necessary to keep the noise contributions from the following stages negligible. On the other hand, the high gain of the first stage limits the tolerance to the input offsets. For these reasons the preamplifier has been divided into two stages which are AC coupled (Fig. 4.6).

The first stage is a simple differential amplifier (transistors M1 to M4) with the feedback resistor R_1 = 100 kΩ. The gain of this part is controlled by the current IPRE. The second stage is formed by a source follower (transistors M10 and M11) and a common source amplifier (transistors M12 and M13) with source degeneration R_2 = 6 kΩ. The gain

of the common source amplifier is fixed and is equal to 5 V/V. Both stages are AC coupled with the capacitor C_S = 4 pF. Because of the very high input resistance of the source follower together with its biasing circuit (transistors M6 to M9), the lower cut-off frequency of this AC coupling circuit is in the range of a few mHz (see section 4.3.3). The total gain of the preamplifier is given as

$$K_v \approx \frac{1}{2} g_{m1} R_1 \frac{g_{m12}}{g_{m13}\left(1 + g_{m12} R_2\right)} \tag{4.1}$$

where:

g_{m1}, g_{m12}, g_{m13} – gate transconductances of transistors M1, M12 and M13,
R_1, R_2 – values of the corresponding resistors shown in Figure 4.6.

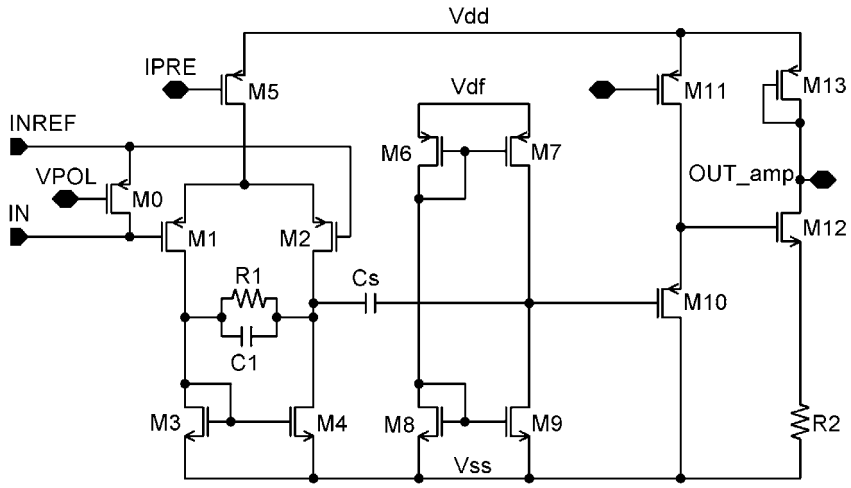

Fig. 4.6. Scheme of the preamplifier

In the frequency range adequate for the retinal signals the noise performance of the CMOS amplifier is usually limited by both noise sources: the 1/f and the white noise. At the lower frequency range the 1/f noise is dominant, whereas at higher frequencies attention should be paid to the white noise too, especially for low bias currents for which the transconductance of the transistor is low and the thermal noise of the channel is relatively high. Since we discuss the noise performance of the CMOS amplifier in the band 20 Hz to 2000 Hz with some constraints on the power dissipation, both components of noise should be taken into account. For the differential amplifier the equivalent input noise is given as follows [103]

$$\frac{\overline{dv_{n\_dif}^2}}{df} = \frac{\overline{dv_{n1}^2}}{df} + \frac{\overline{dv_{n2}^2}}{df} + \frac{g_{m3}^2}{g_{m1}^2}\left(\frac{\overline{dv_{n3}^2}}{df} + \frac{\overline{dv_{n4}^2}}{df}\right) \tag{4.2}$$

where:

$\overline{\frac{dv_{n1}^2}{df}}$, $\overline{\frac{dv_{n2}^2}{df}}$, $\overline{\frac{dv_{n3}^2}{df}}$, $\overline{\frac{dv_{n4}^2}{df}}$ – power spectral densities of equivalent input voltage noise of transistors M1, M2, M3 and M4,

g_{m1}, g_{m3} – gate transconductances of transistors M1 and M3.

It has been assumed that $g_{m1} = g_{m2}$ and $g_{m3} = g_{m4}$. In the above formula the thermal noise of the feedback resistor R_1 and the noise of current source M5 have been omitted, since in our case they are negligible. Formula (4.2) shows that the input transistors M1 and M2 contribute to the total input noise directly, while the contributions of the load transistors M3 and M4 are reduced by the square of the ratio of their transconductances to the transconductance of the input transistor.

For most of CMOS processes the 1/f noise in the PMOS transistors is lower compared to the NMOS transistors. In the chosen MIETEC 0.7 μm technology the 1/f noise coefficient K_{fn} of the NMOS transistors is more than an order of magnitude higher than noise coefficient K_{fp} of the PMOS transistors. On the other hand, for a given bias current and given dimensions of the transistors, the NMOS devices offer larger transconductances and consequently lower white noise. Because of the low frequency region considered in this design the PMOS devices in the input stage have been used. Taking into account the flicker noise only (see formula (2.12)), one can rewrite formula (4.2) as

$$\overline{\frac{dv_{1/f\_dif}^2}{df}} = \frac{2K_{fp}}{C_{ox}W_1L_1}\left(1+\frac{\mu_n K_{fn}L_1^2}{\mu_p K_{fp}L_3^2}\right)\frac{1}{f} \tag{4.3}$$

where:

K_{fn}, K_{fp} – flicker noise constants for NMOS and PMOS transistors,
C_{ox} – oxide capacitance per unit area,
W_1 – width of transistor M1,
L_1, L_3 – lengths of transistors M1 and M3,
μ_n, μ_p – mobility in the channel of NMOS and PMOS transistors,
f – frequency.

The input 1/f noise of the amplifier is inversely proportional to the gate area of the input transistor. The gate length of the input transistor is, however, limited as the contribution of the load transistors is proportional to the ratio L_1/L_3. It can be shown [85] that the minimum of the 1/f noise spectral density is obtained for the L_1/L_3 ratio fulfilling the relation

$$\frac{L_1}{L_3} = \sqrt{\frac{K_{fp}\mu_p}{K_{fn}\mu_n}} \tag{4.4}$$

For the parameters of the chosen process the formula (4.4) yields an optimum ratio L_1/L_3 about 10, for which the flicker noise contributions from input and load transistors are the same.

Although in the low frequency region the thermal noise of the channel is of secondary importance it cannot be completely ignored. In order to optimise the overall noise performance of the amplifier, the optimisation of the 1/f noise should be followed by the proper optimisation of the white noise. Larger transconductance of the transistors offers lower white noise. Let us assume that the transistors work in strong inversion region and then from the formulae (2.3), (2.14) and (4.2) the input referred thermal noise can be written as

$$\frac{\overline{dv_{th\_dif}^2}}{df} = \frac{16}{3}\frac{kT}{g_{m1}}\left(1+\frac{g_{m3}}{g_{m1}}\right) \tag{4.5}$$

The second term in the bracket represents the contribution of thermal noise of the load transistors. Taking all these constraints into account, together with the limit on the transistor area, the dimensions of the input transistors as W_1/L_1 = 1500μm/2μm, and of the load transistors as W_3/L_3 = 100μm/24μm have been chosen. For the above dimensions the white noise in the differential pair is dominated by the thermal noise of the input transistors and formula (4.5) can be reduced to

$$\frac{\overline{dv_{th\_dif}^2}}{df} \approx \frac{16}{3}\frac{kT}{g_{m1}} \tag{4.6}$$

The design of the source follower (transistors M10 and M11) and of the second stage amplifier (transistors M12 and M13) is optimised to meet the linearity requirements. As the input stage has already significant gain, the noise performance of the source follower is not very critical, however, it cannot be completely ignored. The noise calculated at the input of the source follower can be written as

$$\frac{\overline{dv_{n\_sf}^2}}{df} = \frac{\overline{dv_{n10}^2}}{df} + \frac{g_{m11}^2}{g_{m10}^2}\frac{\overline{dv_{n11}^2}}{df} \tag{4.7}$$

where:

$\frac{\overline{dv_{n10}^2}}{df}$, $\frac{\overline{dv_{n11}^2}}{df}$ – power spectral densities of equivalent input voltage noise of transistors M10 and M11,

g_{m10}, g_{m11} – gate transconductances of transistors M10 and M11.

For the flicker noise the above formula gives

$$\frac{\overline{dv_{1/f\_sf}^2}}{df} = \frac{K_{fp}}{C_{ox}W_{10}L_{10}}\left(1+\frac{\mu_n K_{fn} L_{10}^2}{\mu_p K_{fp} L_{11}^2}\right)\frac{1}{f} \tag{4.8}$$

while for the thermal noise in strong inversion one obtains

$$\frac{\overline{dv_{th\_sf}^2}}{df} = \frac{8}{3} kT \frac{1}{g_{m10}} \left(1 + \frac{g_{m11}^2}{g_{m10}^2} \right) \tag{4.9}$$

where:

W_{10} – width of transistor M10,
L_{10} , L_{11} – lengths of transistors M10 and M11,
g_{m10}, g_{m11} – transconductances of transistors M10 and M11.

In the source follower the contributions of the active transistor M10 and the load transistor M11 to the total input noise are described by similar formulas like for the differential pair (smaller by factor 2, see equations (4.3) and (4.5)). The requirements concerning the transconductances of those two transistors are contradictory. The white noise contribution of the active transistor is inversely proportional to its transcoductance while the contribution of the load transistor is proportional to its transconductance. These relations impose contradictory requirements on the sizes and bias currents of the two transistors. Optimising carefully both aspects we have arrived at a solution with W_{10}/L_{10} = 80μm/4μm and W_{11}/L_{11} = 10μm/20μm and both transistors biased with a drain current of 5 μA.

The noise of the circuit which provides the DC bias for the input of the source follower is negligible, due to zero current flowing through the voltage divider formed by transistors M7 and M9 (see section 4.3.3). The noise optimisation of the common source amplifier is very similar to the differential amplifier. In that stage the g_{m12} should be high enough to keep its noise negligible compared with other noise sources. Tuning other components of this circuit, i.e. transistor M13 and resistor R_2 is made to fulfil the requirement of wide linear range at the output of the preamplifier.

There is also another problem which should be solved for the preamplifier stage and that is related to the PMOS transistor M0 placed at the input of a differential pair (Fig. 4.6). This transistor has been implemented for two purposes: to control the input differential resistance of the preamplifer and to provide the possibility of implementing AC coupling between the electrodes and the input of the NEURO64 chip. The PMOS transistor has the dimensions of W_0/L_0 = 3μm/563μm and works in the linear region as a resistor. The external reference voltage VPOL sets its effective resistance precisely over the range from 8 MΩ to 150 MΩ or this resistance can be set practically to infinite value by switching off the transistor. The input resistance of the preamplifier must be kept high due to the relatively high internal resistance of the signal source which is determined by the contact resistance between the neuron cell and the electrode. Depending on the experimental set-up, this contact resistance can be in the range of tens of kΩ to several MΩ [90, 92]. On the other hand, the small signal drain-source resistance of M0 is a source of thermal noise and its high value has a negative influence on a possible crosstalk between the channels in a multichannel system.

Even if we agree to a compromise concerning the noise performance of the preamplifier, it may occur that in some neurobiological experiments input offsets are much higher compared with what our circuit can tolerate with DC coupling to the electrodes. Therefore, the possibility of implementing AC coupling between the electrodes and the input of the

NEURO64 chip is foreseen. In fact, this is the solution commonly used in many experiments. The voltage controlled resistor at the input provides the possibility to control the time constant of the input CR circuit. For the resistor value of 150 MΩ the required lower cut-off frequency of the order of 10 Hz can be achieved for the capacitance value of about 100 pF which is feasible to be implemented on silicon.

4.3.2. Experimental optimisation of operation condition for the preamplifier stage

The gain of the preamplifier is controlled by the current in the input differential pair. A larger drain current in the input transistor M1 (or M2) $I_{DS} = I_{DS1} = I_{DS2}$ results in a larger transconductance g_{m1} of this transistor and according to formula (4.1) in a higher gain. The measured gain as a function of the drain current is shown in Figure 4.7. The measurements have been taken for the reference input connected to 0 V and the supply voltages ±2.5 V.

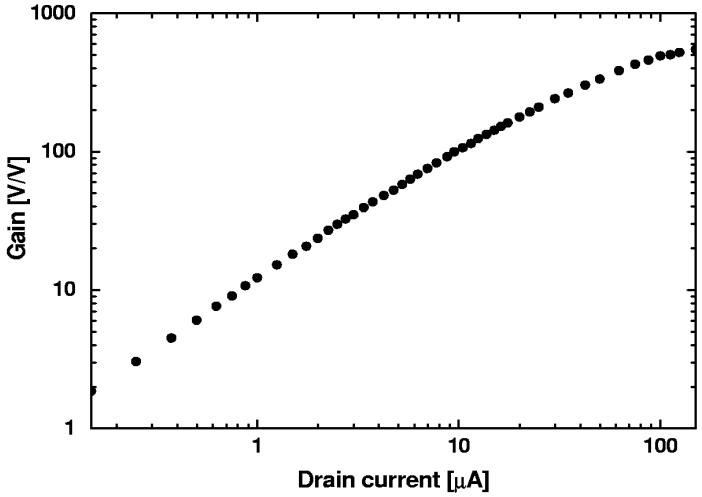

Fig. 4.7. The measured gain of the preamplifier as a function of the drain current I_{DS} in the input transistors

From the plot in Figure 4.7 one can see different dependence of the gain vs drain current for the low and high values of the current. As the bias current in the second stage is fixed, the only factor in the equation (4.1), which varies with the drain current in the input transistors is the transconductance g_{m1}. Thus, the dependence of the gain on the bias current illustrates the dependence of the transconductance of the input transistors on the drain current. It is well known that in a weak inversion region the transconductance is proportional to the current, while in a strong inversion it becomes proportional to the square root of the current.

To distinguish between weak and strong inversion regions one can use the method proposed in [104]. The transconductance to current ratio is expected to be constant in the weak inversion, while the transconductance to square root of current ratio is expected to be constant in the strong inversion region. Since in our case the measured gain is proportional

to the transconductance of the input transistor, the behaviour of the gain to current ratio and the gain to square root of current ratio illustrates the behaviour of the transconductance. The corresponding plots normalised to their maximum values are shown in Figure 4.8. From the plot shown in Figure 4.8 it becomes clear, that the change of the drain current in the range as illustrated in Figure 4.7 causes that the input transistors operate in weak or moderate or strong inversion. This is a result of the noise optimisation, which has led us to large ratio of width to length of the input transistors (W_1/L_1 = 1500μm/2μm).

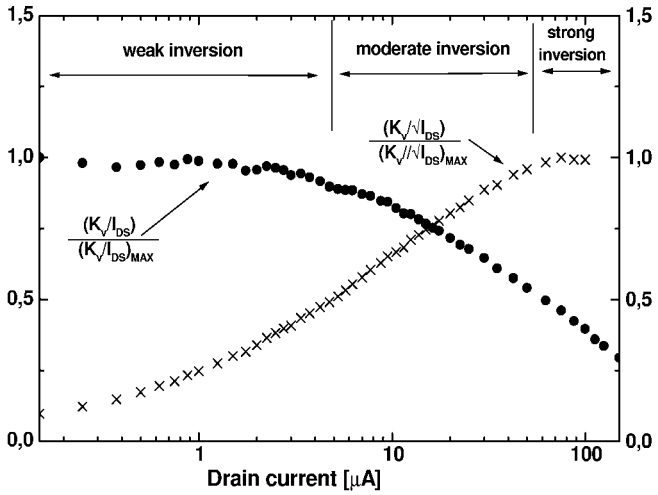

Fig. 4.8. Gain to current ratio and gain to square root of current ratio (normalised to their maximum values) vs drain current

The change of current in the input stage is limited by power consumption and noise performance of the circuit. In order to avoid noise contribution from successive stages, one requires the gain to be at least 50 V/V, which is obtained for the input transistor bias current above 5 μA. On the other hand, the bias current is limited by the power consumption which should not exceed 1 mW for the preamplifier stage and preferably it should be lower. Thus, the maximum value of the bias current in each of the input transistors is 100 μA.

To evaluate the noise performance of the preamplifier we have measured the full spectra of the equivalent input noise for different bias conditions of the input transistors. The examples of such spectra for three different drain currents in the input transistor are shown in Figure 4.9. In order to separate the flicker and thermal noise contributions the measured noise spectra have been fitted to the formula

$$\frac{\overline{dv_n^2}}{df} = \frac{A_1^2}{f} + A_2^2 \tag{4.10}$$

with the parameters A_1 and A_2. Having both parameters we can calculate the noise corner frequency f_c for each bias current.

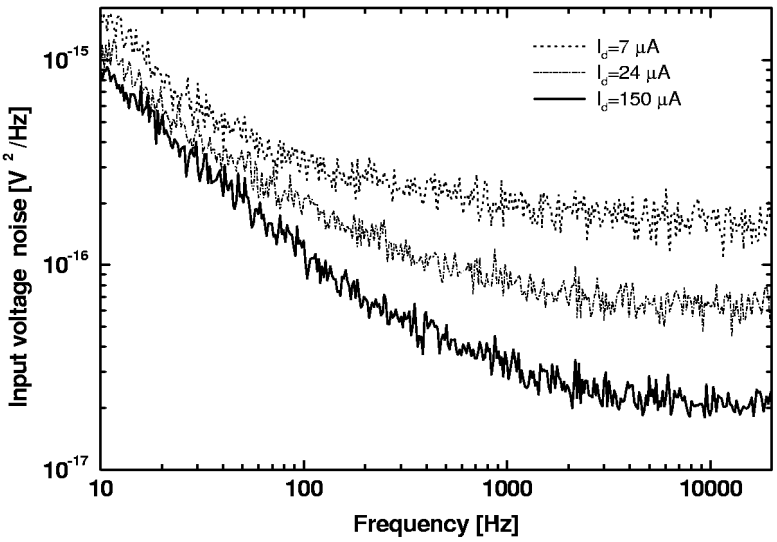

Fig. 4.9. Power spectral density of the equivalent input voltage noise for different drain currents in the input transistors

The measured noise spectra have been integrated over the frequency range from 10 Hz to 20 kHz and the rms values of the input noise have been calculated as a function of the transistor bias current. The results of the noise measurements for different values of drain current in the input transistor are summarised in Table 4.1. An increase of noise is observed with the decreasing current I_{DS} in the input stage. The value of rms noise increases 2.5 times for the lowering of I_{DS} from 150 μA to 7 μA, which is caused by two effects. The first one is the increase of the white noise. If we check how the parameter A_2 depends on the current, we can see that for lowering the current from 150 μA to 7 μA the parameter A_2 increases also about 2.5 times.

Secondly, at a lower gain of the input differential stage the noise contribution from the following source follower and the common source amplifier becomes non-negligible. The noise measurements of the second stage itself show, that for the lowest value of the I_{DS} current, as listed in Table 4.1, the second stage contributes about 10% to the total noise of the preamplifier. One can notice that by proper designing the 1/f noise is indeed low, so that the corner frequency is below 400 Hz. Parameter A_1 in the Table 4.1, which is responsible for the level of the 1/f noise, is only slightly dependent on the transistor bias current and this is in agreement with flicker noise modelling (see chapter 2.1.2).

There is also another aspect which should be taken into account in this design. The gain of the differential stage determines the tolerance of the amplifier to the input offsets. In order to evaluate this parameter we have applied the sine wave of amplitude 500 μV with the DC level at 0 V to the input IN (Fig. 4.6), and measured the gain as a function of the DC offset applied to the INREF input. The tolerance to the input offset is defined as the value of input offset for which the gain is reduced by 5% with respect to nominal value (with zero offset). The obtained results are shown in Figure 4.10.

Table 4.1
Summary results of input noise measurements

I_{DS} μA	Noise rms μV rms	A_1 V	A_2 nV/√Hz	f_c Hz
7	1.82	11.5e-8	12.8	81
10	1.46	11.4e-8	10.3	121
16	1.32	10.4e-8	9.6	118
22	1.16	10.3e-8	8.5	147
33	1.11	10.3e-8	7.7	181
43	0.99	10.0e-8	6.9	211
63	0.82	9.5e-8	6.0	253
79	0.80	9.9e-8	5.3	350
100	0.76	9.4e-8	5.2	329
150	0.72	9.5e-8	5.0	360

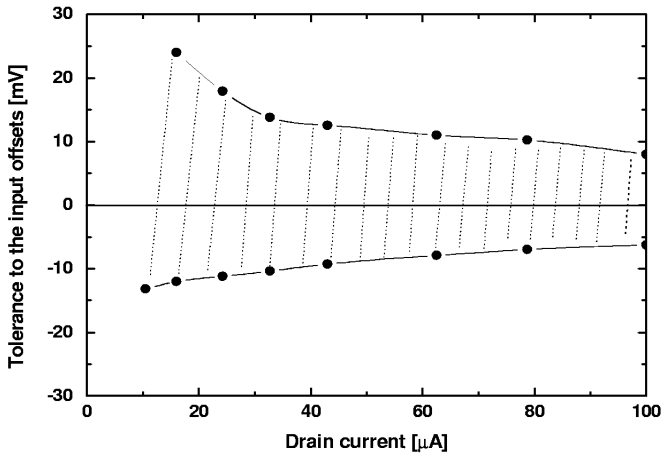

Fig. 4.10. The measured tolerance to the input offsets as a function of the bias current

4.3.3. AC coupling circuit

As discussed in the previous section, we need to separate the gain stages in the preamplifier by an AC coupling circuit in order to avoid full amplification of the input offsets and to make the circuit tolerable to a certain level of these offsets. The offset problem appears also at the output of the filter stages, due to transistor matching. In a multichannel IC with the multiplexing of the output signals from many channels, a small channel-to-channel offset spread simplifies the design of the multiplexer and reduces the requirements concerning the resolution of an ADC used for measuring the signals. For these reasons AC couplings are also needed in the filter stages which follow the preamplifier.

In order to keep the value of the coupling capacitance within a reasonable range of a few pF, one needs a very high input resistance of the source follower including the biasing circuit. The bias of the input source follower is provided by the voltage divider built of

output resistances of two current sources M7 and M9 (Fig. 4.6). The dimensions *W/L* of the transistors employed in the current sources are 5μm/100μm and 5μm/265μm for the PMOS and NMOS transistors respectively. In the case of perfect matching of the transistor pairs M6–M7 and M8–M9, the transistors M7 and M9 stay in saturation and guarantee a very large input resistance of the whole circuit. However, for the transistors biased in strong inversion a small mismatch in the current mirrors causes one of the transistors, M7 or M9, to move from the saturation region into the linear region and then the input resistance of the circuit decreases rapidly. The negative effect of the mismatch can be reduced significantly when the transistors are biased in the weak inversion. Although matching of the drain currents is worst in the weak inversion compared with the strong inversion bias condition [53], the sensitivity of the operating point of our circuit to the relative changes of the drain current is much lower in the weak inversion compared with the strong inversion. The effect of the mismatch is illustrated in Figure 4.11.

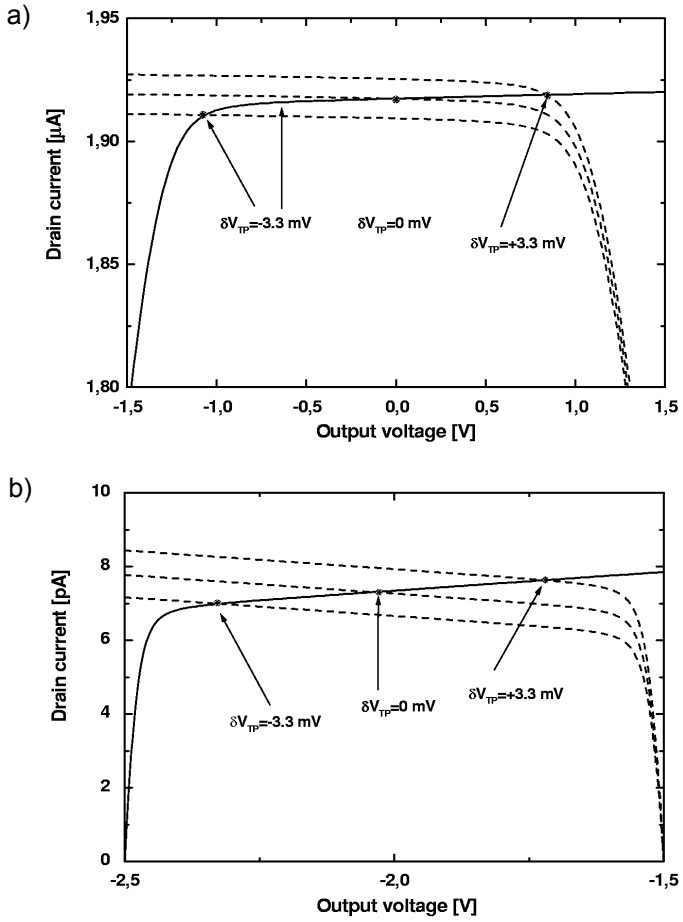

Fig. 4.11. DC output characteristic of the voltage divider: a) biased in strong inversion; b) biased in weak inversion

The plots show the output characteristics of the two transistors used in the voltage divider, assuming the mismatch of the threshold voltages in the PMOS current mirror to be of ± 3.3 mV at 3 sigma level. This expected level of mismatch is based on the matching data of the process used and the dimensions of transistors implemented in the design. For the circuit biased with $V_{df} - V_{ss}$ = 5 V (Fig. 4.6) the transistors work in strong inversion and the operating point of the voltage divider is extremely sensitive to the matching of transistors in the current mirrors, as shown in Figure 4.11a. For the bias voltage V_{df} low enough the transistors are biased in weak inversion and, as shown in Figure 4.11b for $V_{df} - V_{ss}$ = 1 V, for the same mismatch both transistors stay in saturation providing high output resistance of the voltage divider.

The voltage divider is biased from a separate reference voltage V_{df} in order to ensure that the transistors work in the saturation region regardless of the process variations. The measurements have shown that the circuit works satisfactorily for the bias $V_{df} - V_{ss}$ = 0 V. The input resistance of the voltage divider is then of the order of a few TΩ and, with the coupling capacitance C_s = 4 pF, provides a lower cut-off frequency of the order of a few mHz. The voltage gain of the complete source follower is about 0.95 V/V. The performance of the circuit is illustrated in Figure 4.12, which shows 10 mHz sine-wave signal recorded at the input of the AC coupling circuit and at the output of the source follower. Linearity range measured for the bias $V_{df} - V_{ss}$ = 0 V at the frequency of 8 Hz is 500 mV_{pp} for the total harmonic distortion smaller than 1%.

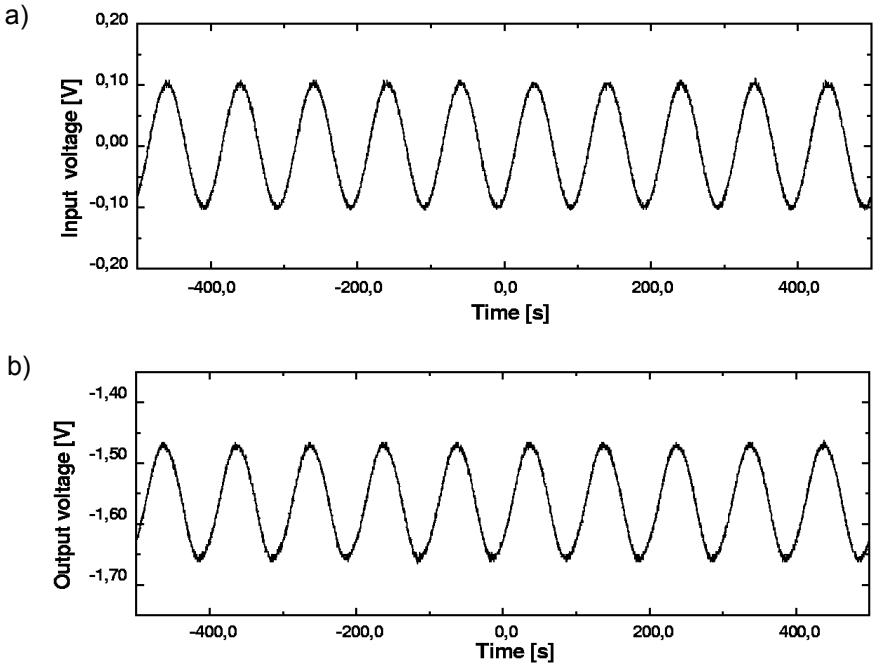

Fig. 4.12. Sine-wave signal of 10 mHz frequency: a) recorded at the input of the AC coupling circuit; b) recorded at the output of the source follower

For our applications the lower cut-off frequency of this circuit does not need to be so low and in principle it could be reduced by increasing the V_{df} voltage, and so decreasing the resistance of the voltage divider. The linear range of the circuit increases with the increase of the V_{df}–V_{ss} voltage.

However, increasing the V_{df} –V_{ss} voltage above 0 V results in the non-zero current flowing through the transistors M7 and M9 and in the generation of the 1/f noise in these transistors. In addition, with the increase of the V_{df} –V_{ss} voltage one observes a larger channel-to-channel spread of the DC voltage provided by this voltage divider. Thus, although the increase of the V_{df}–V_{ss} gives a shorter time constant of the coupling circuit, and improves the linearity range, the increase of the noise and offset spread are the limiting factors.

4.3.4. Band-pass filter

The choice of the topology of the band-pass filter stage is dictated by the silicon area and the power consumption constraints. A continuous time RC filter architecture has been chosen as it offers an easy way to build a modular multichannel system. In order to satisfy the requirement for the lower cut-off frequency to be as low as 20 Hz, a novel scheme of the band-pass filter has been developed which requires relatively low value capacitors, in the range of a few pF. These capacitors can be easily implemented on silicon, even in a multichannel chip. In principle, the AC coupling circuit described in the previous sections could be employed as a high-pass filter. However, although the circuit would provide the cut-off frequency of 20 Hz using very small capacitance, the exact cut-off frequency could not be controlled with the required precision.

The circuit diagram of the filter stage is shown in Figure 4.13. At the input of the filter the AC coupling circuit discussed in the previous section has been used. This solution allows one to use simple cascade connections of several filter stages.

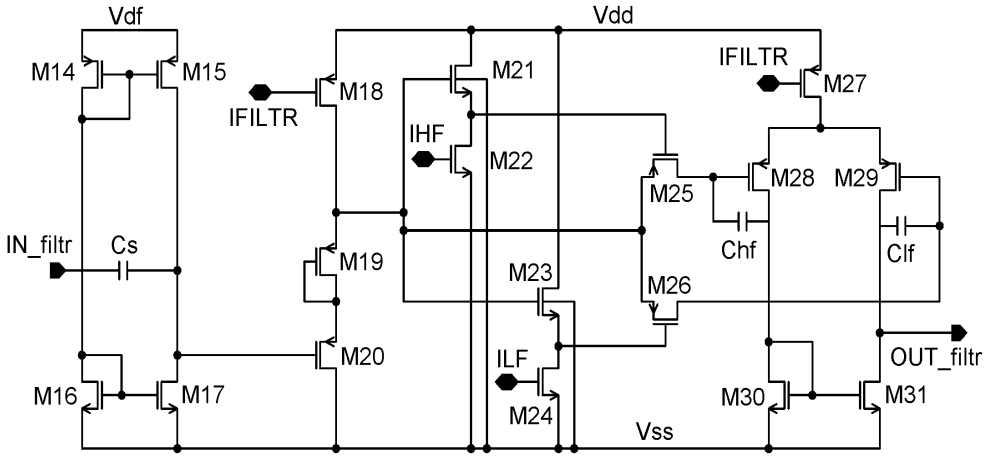

Fig. 4.13. Schematic diagram of the filter stage

The core of the filter is built of transistors M21 to M31. The band-pass filter is obtained as a combination of two RC low-pass filters with the cut-off frequencies corresponding to the required lower and higher cut-off frequency and of a differential amplifier. The resistors of the RC filters are built of transistors M25 and M26, which are biased in the linear region. The effective capacitances are formed by the capacitor C_{hf} for the higher cut-off frequency and by the capacitor C_{lf}, multiplied due to the Miller effect, for the lower cut-off frequency.

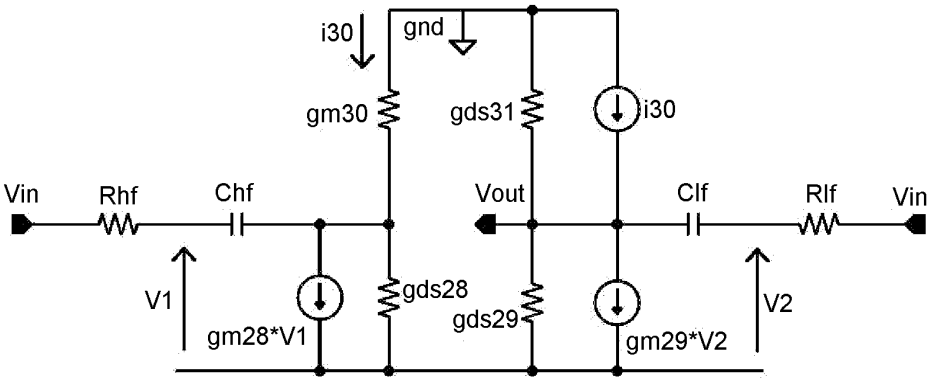

Fig. 4.14. Simplified small signal circuit of the band-pass filter

The small signal analysis of the core part of the filter can be accomplished with assistance of the simplified circuit diagram shown in Figure 4.14. The transistors M25 and M26 are replaced by the resistors R_{hf} and R_{lf} respectively. The output resistance of the current source M27 has been omitted in the scheme assuming that it is sufficiently high. For further simplification the conductance g_{ds30} can be neglected compared with the transconductance g_{m30} of M30. Assuming additionally that both branches of the differential amplifier are perfectly matched we have $g_{m28} = g_{m29}$ and $g_{ds28} = g_{ds29}$.

The analysis of the small signal model (see Appendix IV), after some algebra and discarding minor terms, results in the following transfer function

$$K_v(s) \approx K_0 \frac{s\left(1 - \frac{s}{z_2}\right)}{\left(1 - \frac{s}{p_1}\right)\left(1 - \frac{s}{p_2}\right)} \tag{4.11}$$

where K_0, z_2, p_1 and p_2 are given by

$$K_0 = \frac{g_{m29}}{g_{ds29} + g_{ds31}}\left(C_{lf} R_{lf} - C_{hf} R_{hf}\right)$$

$$z_2 = -\frac{2 g_{m30}\left(C_{lf} R_{lf} - C_{hf} R_{hf}\right)}{C_{lf} C_{hf}\left(R_{lf} + R_{hf}\right)} \tag{4.12}$$

$$p_1 = -\frac{1}{\frac{g_{m29}}{g_{ds29} + g_{ds31}} C_{lf} R_{lf}}$$

$$p_2 = -\frac{1}{C_{hf} R_{hf}}$$

where:

C_{lf}, C_{hf}	–	values of corresponding capacitors in Figure 4.14,
R_{lf}, R_{hf}	–	values of corresponding resistors in Figure 4.14,
g_{m29}, g_{m30}	–	transconductances of transistors M29 and M30,
g_{ds29}, g_{ds31}	–	source-drain conductances of transistors M29 and M31.

The filter transfer function has two zeros (the first one at 0 Hz and the other one z_2 at high frequency) and two poles p_1 and p_2. The dominant pole p_1 of the filter, which determines the lower cut-off frequency, is pushed down by the Miller effect. The capacitance C_{lf} = 4 pF in the pole p_1 is multiplied by the gain of the differential amplifier $K_{vd} = g_{m29}/(g_{ds29}+g_{ds31})$, which can be tuned by external current in the range from 200 V/V to 400 V/V. The capacitance C_{hf} of 5 pF in the pole p_2 is not multiplied, as it is connected to the low gain output node of the differential amplifier. The resistors R_{lf} and R_{hf}, which are discussed in detail below, can be tuned by external reference currents in the range from a few MΩ to a few tens of MΩ. In this way one can control the band of the filter over a relatively wide range. For a wide filter band, when $|p_1| << |p_2|$ and $|p_1| << |z_2|$, one obtains from equations (4.11) and (4.12) the gain of the filter as

$$\left|K_v(s)\right| \approx \left|1 - \frac{C_{hf} R_{hf}}{C_{lf} R_{lf}}\right| \tag{4.13}$$

In our design the capacitances C_{lf} and C_{hf} are of the same value and the gain depends only on the ratio of the resistor values R_{lf}/R_{lf}. The wide band setting from 11 Hz to 2800 Hz, as required for some applications, is obtained for the resistor values R_{hf} = 14 MΩ and R_{lf} = 8.5 MΩ which give the gain of 0.65 V/V. Bringing the two poles closer results in some increase of the gain up to the maximum value for $|p_1| = |p_2|$. Assuming that the condition $|p_1| << |z_2|$ is fulfilled, the gain of the filter can be obtained as

$$\left|K_v(s)\right| \approx \frac{1}{\sqrt{2}}\left|1-\frac{C_{hf}R_{hf}}{C_{lf}R_{lf}}\right| \tag{4.14}$$

The equality of the two poles is obtained by tuning appropriately the values of the resistors R_{hf} and R_{lf}. Thus, requiring that the poles p_1 and p_2 given by formula (4.12) should be equal, equation (4.14) can be rewritten in the form

$$\left|K_v(s)\right| \cong \frac{1}{\sqrt{2}}\left|1-\frac{g_{m29}}{g_{ds29}+g_{ds31}}\right| \tag{4.15}$$

For our design formula (4.15) gives the ultimate value of gain equal to 282 V/V. In practice the maximum value is lower because the condition $|p_1|=|p_2|$ is never fulfilled exactly.

In order to obtain long RC time constants of the filter using capacitors of the values which are practical for the implementation on silicon, large value resistors are needed, even if the Miller effect is employed for the capacitance multiplication as it is done in our design. The resistors are built as the long PMOS transistors M25 and M26 of the dimensions W_{25}/L_{25} = 3µm/500µm and W_{26}/L_{26} = 3µm/300µm respectively. The transistors are biased in the linear region with V_{DS} = 0. The most critical aspect of this solution is the linearity of the resistors as the signal levels in the filter stages can be up to 1 V_{pp}. The nonlinearity of the MOSFET characteristic can be cancelled by the proper use of fully balanced bias networks [105]. This solution is not very practical if the resistors to be controlled by external reference voltage or current are required. For the NEURO64 another solution based on a dynamic bias of the transistors M25 and M26 has been implemented. The input signal is applied simultaneously to the sources of these transistors and with a DC offset to the gates. The DC offsets providing the bias for these transistors are controlled by the external currents ILF and IHF. This solution allows one to control the output resistance of the transistors M25 and M26 in the range from a few MΩ to a few tens of MΩ, while maintaining their characteristics linear over the required range.

In summary, taking into account the results of the above analysis one can define three different ways in which the band of the filter can be controlled. The three different possibilities are illustrated in Figure 4.15 by the examples of the measured frequency response characteristics of two cascaded filter stages:

- the centre frequency of the filter can be tuned by the currents IHF = ILF = var without affecting the gain (Fig. 4.15a);
- the lower cut-off frequency can be tuned through the differential gain K_{vd} in the filter stage controlled by the IFILTR current (Fig. 4.15b);
- the lower and/or the higher cut-off frequency can be tuned independently by the control currents ILF and/or IHF; however, for this configuration the gain of the filter stage changes with the moving of the cut-off frequencies (Fig. 4.15c); the possibility of tuning the band and the gain of the filter appears to be useful for the setting-up and optimising neurophysiological experiments as quite often the parameters of the neuronal signals are not well known.

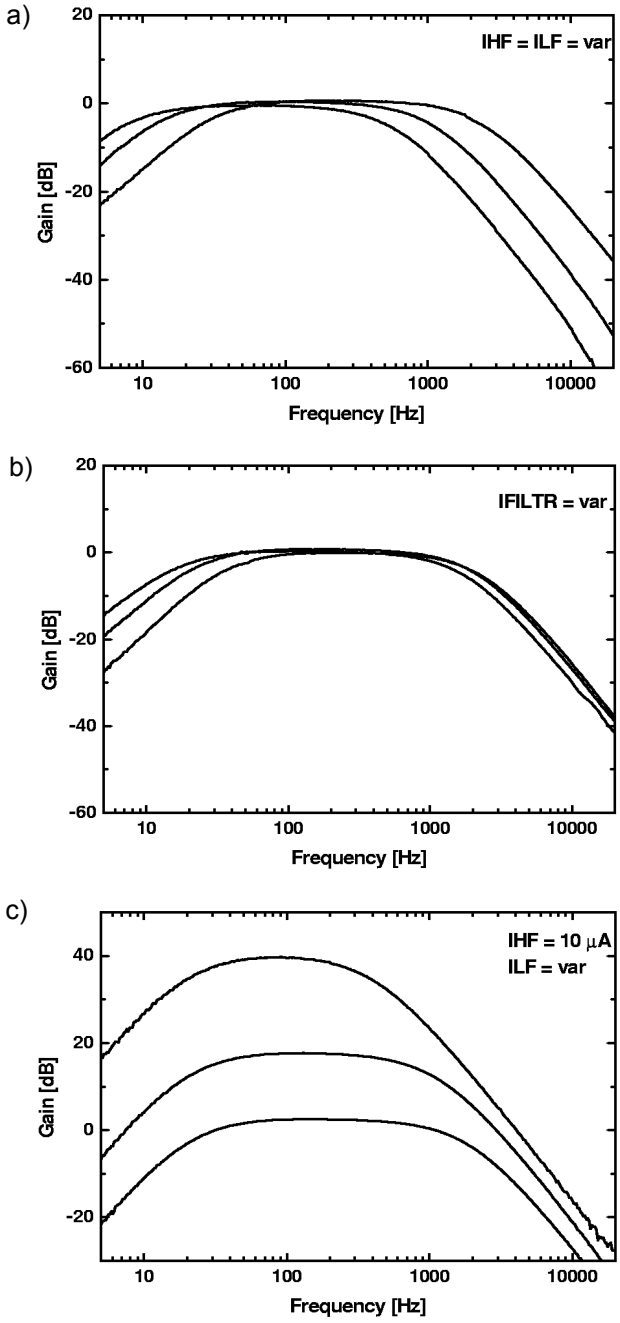

Fig. 4.15. Measured frequency response of a single filter stage: a) IHF = ILF = var; b) IFILTR = var; c) IHF = 10 μA, ILF = var

As a consequence of the employed structure of the filter one thing should be kept in mind, namely a relatively high noise of this circuit. The two series resistors R_{hf} and R_{lf} connected to the inputs of the differential amplifier are significant noise generators. Therefore, in order to keep the noise contribution of the filter stage negligible one cannot reduce the gain of the preamplifier below a certain value. The noise analysis of the filter stage can be performed using the simplified equivalent circuit shown in Figure 4.14. The dominant contributions to the noise at the filter output come from the transistors M25 and M26 which work as linear resistors R_{hf} and R_{lf}. Because these transistors work with I_{DS} = 0, they generate only white noise which can be described as a thermal noise of the channel resistance. The two noise sources contribute to the output noise according to the following formula

$$\frac{\overline{dv_{th25}^2}}{df} = \left| K_{vd} \frac{(1+sC_{lf}R_{lf})}{\left(1-\frac{s}{p_1}\right)\left(1-\frac{s}{p_2}\right)} \right|^2 4kTR_{hf}$$

$$\frac{\overline{dv_{th26}^2}}{df} = \left| K_{vd} \frac{-1}{\left(1-\frac{s}{p_1}\right)} \right|^2 4kTR_{lf} \tag{4.16}$$

where p_1 and p_2 are given by equations (4.12) and $s = j\omega$. From the above equation one can see that for very low frequencies, below the lower cut-off frequency of the filter, the noise from M25 and M26 is transferred to the output with the full open loop gain K_{vd}^2 because in this frequency range the feedback is not active. The noise of the transistors M28–M31 in the differential stage is then dominated by the 1/f noise and for that reason the design has been optimised in a similar way as described in the section 4.3.1 for the preamplifier. For frequencies below the lower cut-off frequency the transfer functions for the noise sources of the transistors M28–M31 are the same as in an ordinary differential pair. For frequencies above the lower cut-off frequency the noise contributions to the output noise are reduced because for each of the transistors M28–M31 the transfer function of noise has a dominant pole $p_1 = A_{vd} C_{lf} R_{lf}$.

The spectral densities of noise measured at the output of a single filter stage and at the output of two cascaded filter stages are shown in Figure 4.16. The gain for the filter centre frequency is set to 0 dB, while the lower and the higher cut-off frequencies are 74 Hz and 4.2 kHz respectively for a single filter stage. For two cascaded filter stages the total gain is 0 dB, while the lower and the higher cut-off frequencies are 120 Hz and 2.8 kHz respectively.

The plots in Figure 4.16 show clearly that in the low frequency range, below the lower cut-off frequency, the noise is dominated by the white noise of resistors R_{hf} and R_{lf}. Within

the band of the filter the noise decreases by 40 dB/decade as expected according to the formula (4.16). For two cascaded filter stages one observes some additional contribution of noise from the second filter within the filter band which is expected because the gain of each filter is set to 0 dB.

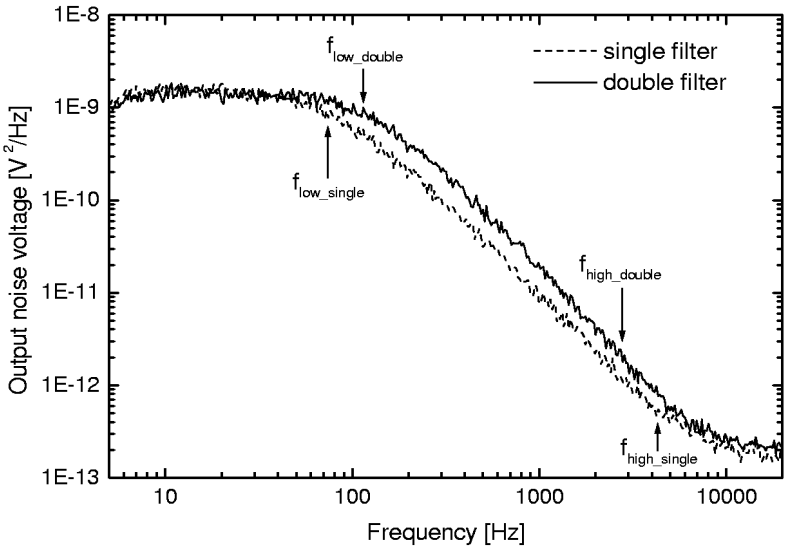

Fig. 4.16. Noise spectrum measured at the output of a single filter stage and at the output of two cascaded filter stages

4.3.5. Output amplifier

The main purpose of the output stage in the NEURO64 design is to reduce the channel-to-channel variation of the DC output offset from the filter stage. The schematic diagram of the output amplifier is shown in Figure 4.17. It employs a replica of the bias circuit and a differential output stage. The input stage is built of two source followers, identical to the source followers in the filter stage. The additional source follower provides only the bias for the inverting input of the differential pair which works with the local feedback resistor R_3 = 60 kΩ.

The critical parameter of this stage is the linearity because of the large output signals. The design has been tuned is such a way that the gain of the output amplifier is equal to 2, the output DC level is near 0 V and the output linear range is +/−1V. For these conditions the spread of the DC output offset is typically about 5 mV rms. For the gain of the whole chain of 1000 V/V, the equivalent input offset spread of 5 μV rms is comparable with the value of the equivalent input noise measured within the band defined by the filter. The output resistance of this stage is 4.4 kΩ.

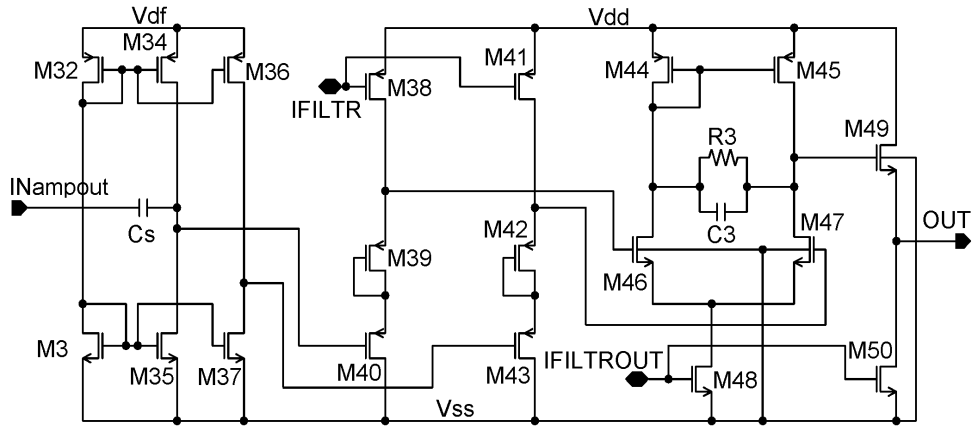

Fig. 4.17. Schematic diagram of the output amplifier

4.4. Analogue multiplexer

In order to reduce the number of output lines, the 64 analogue signals from the 64 front-end channels on the chip are multiplexed to a single output by an analogue multiplexer. The band of the front-end electronics is limited to 2 kHz by the second-order continuous time filters. To omit aliasing problem, it has been assumed that the sampling rate of the single channel should be about 20 kHz. For the 64 channel chip the minimum requirement concerning the multiplexing rate is 64 × 20 kHz = 1.28 MHz. The data from the chip are sent to the data acquisition system based on a commercially available flash ADC plugged into a personal computer [106]. This card includes four ADC channels with 5 MS/s simultaneous sampling rate capability and 12-bit resolution. Because the final system will consist of several hundred of channels it has been assumed that the multiplexer should be able to work with a 5 MHz clock, and then a single 5 MHz ADC can serve 256 readout channels.

A block diagram of the multiplexer is shown in Figure 4.18. The multiplexer is controlled by three external digital signals: *HOLD_ext*, *CLOCK_ext* and *RESET_ext*. All of them are applied in the differential mode using the LVDS levels to reduce the pick-up of digital noise by the sensitive analogue circuits. The readout cycle is started by the *RESET_ext* signal which resets all logic blocks and connects hold capacitors CH0–CH63 and CHD via transmission gates SH0–SH63 and SHD to the outputs of the front-end channels (acquisition mode).

The rising edge of the *HOLD_ext* signal switches off the gates SH0–SH63 and SHD and the value of the analogue signal from the front-end channels is stored on the hold capacitors CH0–CH63 and CHD (hold mode). The *HOLD_ext* signal is also used to generate a single RINT pulse (one clock period width) in the synchronous READ_INIT CONTROL block. That pulse, passing through the synchronous SHIFT REGISTER, opens and closes sequentially the gates starting from the first SR0 and finishing at the last SR63.

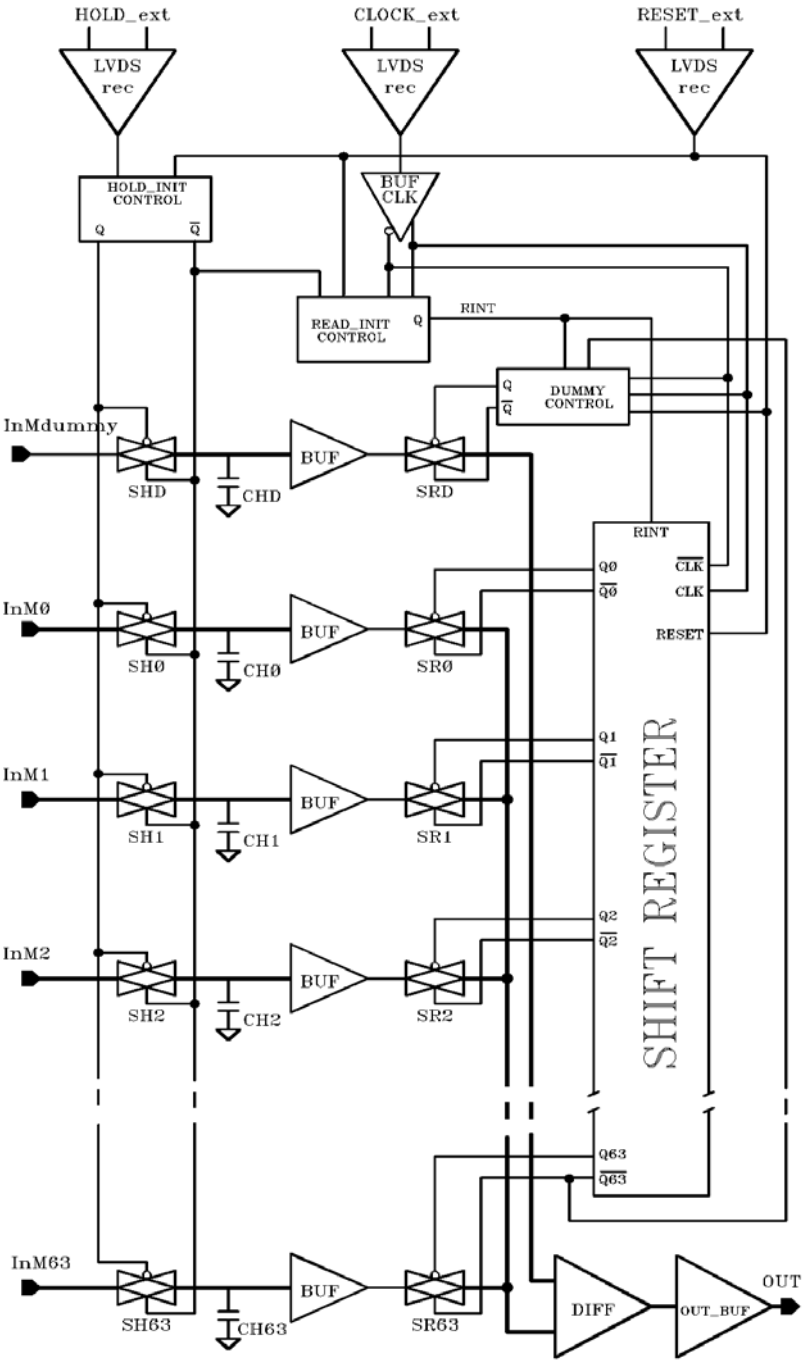

Fig. 4.18. Block diagram of the multiplexer

During the sequential readout of the hold capacitors, the DUMMY CONTROL block keeps the transmission gate SRD switched on and the signal from the dummy channel is subtracted from the signal value from other channels in the DIFF block. This helps to reduce the injection of power supply and clock related noise into the signal path. At the end of the readout sequence the *RESET_ext* signal is applied again, starting the next acquisition sequence.

As mentioned above, the required multiplexing rate in the developed retina readout system is up to 5 MHz, which is not very demanding for a multiplexer design. For speed performance of the multiplexer three time constants should be taken into account:

- time constant τ_{sh} of the sample and hold circuit,
- time constant τ_{sr} at the output of multiplexed switches SR0–SR63 and SRD,
- time constant τ_{out} of the output buffer taking into account external load capacitance.

The settling time of buffers implemented in this particular circuit is of secondary importance.

The sample and hold part is designed in a conventional open-loop architecture [107]. All the switches are built as transmission gates to lower their small signal on-resistance and reduce such effects as charge injection and clock feed-through. The NMOS transistors in the transmission gates SH0–SH63 and SHD have minimal dimensions of W/L = 2μm/0.7μm, while the PMOS transistors have W/L = 5μm/0.7μm. A small signal on-resistance of the transmission gate is in the range from 1.7 kΩ to 3 kΩ depending on the level of the input signal. The capacitors CH0–CH63 and CHD are 2 pF each and together with 0.5 pF input capacitance of buffer BUF give the total hold capacitance about 2.5 pF. The sample and hold circuit is driven by the source follower in the last stage of the front-end channel with output resistance of 4.4 kΩ. The above numbers (4.4 kΩ + 3 kΩ) × 2.5 pF give the time constant of the sample and hold circuit τ_{sh} = 18.5 ns. Since the voltage stored on CH0–CH63 and CHD capacitors during the hold mode can be corrupted by transient current drawn by the following successive circuit, buffer BUF is placed at the output of the sample and hold circuit.

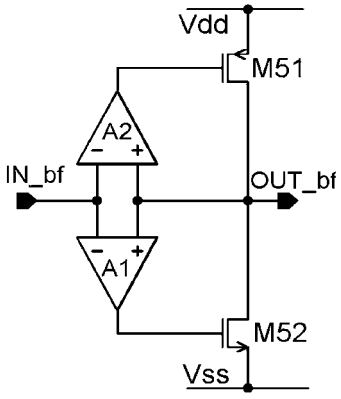

Fig. 4.19. Scheme of the buffer BUF with error differential amplifiers A1 and A2

The buffer BUF (Fig. 4.19) is made as a common source amplifier with negative shunt feedback implemented with error amplifiers A1 and A2. Such a configuration does not

change the DC level and offers good swing characteristic. The output resistance of the buffer is 1.7 kΩ. The transmission gates SR0–SR63 and SRD have a small signal on-resistance in the range from 0.8 kΩ to 1.5 kΩ, because of the larger transistors used. The total capacitance at the output of the switches SR0–SR63 and SRD is a sum of the input capacitance of the DIFF block of 0.2 pF and the parasitic capacitance of 2.4 pF of the metal line connecting the above switches with the DIFF block. The time constant of this part of the multiplexer is τ_{sr} = 8.3 ns (3.2 kΩ × 2.6 pF).

The last stage in the multiplexer is the output buffer OUT_BUF. The output buffer has the same configuration as the buffer BUF (Fig. 4.19). Larger output transistors and larger current in that stage ensure the output resistance of 200 Ω which is low enough to drive load capacitance up to 100 pF with 5 MHz clock.

4.5. Mismatch modelling of multichannel chip

As mentioned in the earlier section, matching of analogue parameters from channel-to-channel is a very critical aspect of the ASIC discussed. To estimate the channel-to-channel matching performance, the Monte Carlo simulations have been done perturbing two BSIM3v3 standard parameters: zero-bias threshold voltage VTH0 and surface mobility U0 (see section 2.3.7). The parameters for the threshold voltage V_{T0} and the current factor β mismatch in the technology used are given according to the following equations

$$\sigma^2(V_{T0}) = \frac{A_{VT0}^2}{WL} + C_{VT0}^2 \tag{4.17}$$

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{A_\beta^2}{WL} + C_\beta^2 \tag{4.18}$$

where the values of the parameters A_{VT0}, A_β, C_{VT0}, C_β are listed in Table 4.2.

Table 4.2
Matching parameter for NMOS and PMOS transistors in 0.7 μm n-well CMOS process for V_{DS} = 3 V, V_{BS} = 0 V

Parameter	NMOS	PMOS	Unit
A_{VT0}	11.5	23	mV μm
A_β	2.5	2.7	% μm
C_{VT0}	0.2	0.4	mV
C_β	0.05	0.04	%

The values of the matching parameters are valid under the assumptions that the matched transistors are drawn in a common centroid layout, with an identical surrounding and no metal 2 cross-over. Formulae (4.17) and (4.18) are slightly different than (2.22) and

(2.27) discussed in chapter 2, because instead of the distance dependent terms there are equivalent constants C_{VT0} and C_β . The n-well resistors used in the preamplifier and the output amplifier stage are drawn in the common centroid layout with dummy structures and no metal cross-over. For these resistors a relative error $\Delta R/R$ of 0.1% at one sigma level has been assumed.

The thin oxide polysilicon-diffusion structure has been used to make the capacitors. The capacitors in the analogue processing chain have a rather large value of 4 pF (for coupling capacitors see Figure 4.5) or 5 pF (for C_{hf}, C_{lf} in the filter stage – Fig. 4.13). These capacitors have the areas equal to 5400 μm^2 and 6700 μm^2 respectively and the relative error $\Delta C/C$ of 0.1% at one sigma level has been incorporated for matching simulations. With the above assumptions one can perform the Monte Carlo analysis using HSPICE to estimate the gain and the cut-off frequencies distributions at the output of a multichannel IC. The results of 100 iterations are presented in Figure 4.20. The ratio of standard deviation (sd.) to the mean value of a given parameter is used for further discussion on matching performance.

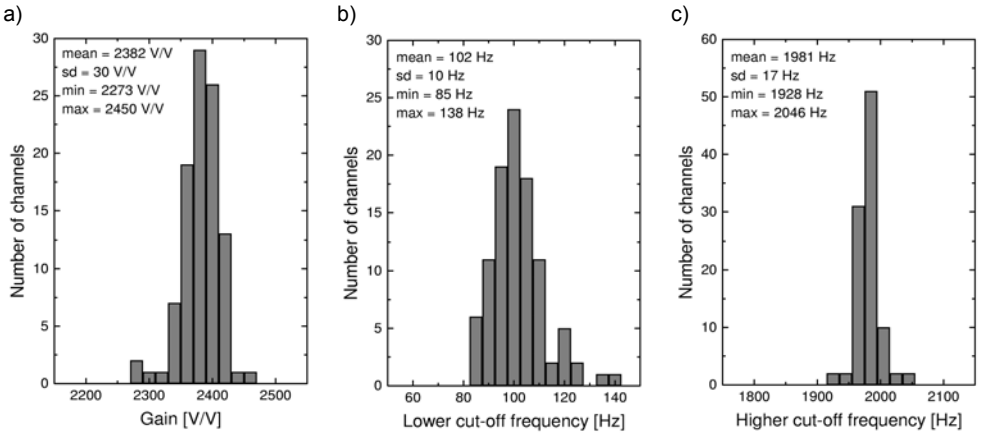

Fig. 4.20. Distributions of analogue parameters at the output of a single channel for 100 iterations of the Monte Carlo matching analysis: a) gain; b) lower cut-off frequency; c) higher cut-off frequency

Conclusions from the Monte Carlo simulations are as follows:

- spread of higher cut-off frequency which depends on C_{hf} and the source-drain resistance of transistor M28 (see section 4.3.4) is small, i.e. sd./mean = 0.86%, which means that the idea of using very long MOS transistors as high resistors is correct,
- spread of lower cut-off frequency is rather high and sd./mean = 9.8%; according to equation (4.12) the lower cut-off frequency depends not only on C_{lf} and R_{lf} but also on the large gain $K_{vd} = g_{m29}/(g_{ds29}+g_{ds31})$ of differential stage M27–M31 (Fig. 4.13); the spread of this gain is due to the mismatch of threshold voltage V_{T0} of the transistors M28 and M29 (W_{28}/L_{28} = 80μm/2μm) and is a main reason of high spread of lower cut-off frequency; the mismatch of V_{T0} generates offsets at the input of the differential stage (chapter 2.3.4) and the high gain of this stage is very sensitive to these offsets,
- spread of gain sd./mean = 1.26% is on an acceptable level and comes from variation of gain in each stage of the analogue chain, and from variation of cut-off frequencies.

4.6. Layout of NEURO64

The layout of the chip is shown in Figure 4.21. The NEURO64 IC has been designed for 0.7 μm CMOS technology on an epi-type substrate process by ALCATEL-MIETEC.

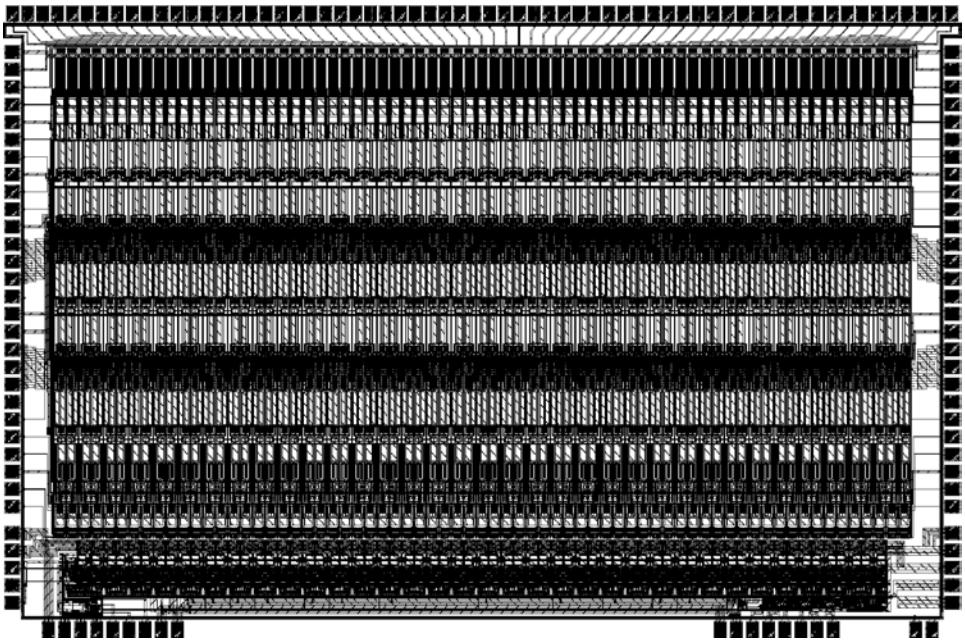

Fig. 4.21. Layout of NEURO64: 64 input pads are on the top , the test and control pads for analogue part on the left and right, the pads for the multiplexer at the bottom

The total area of the chip is 4000×6500 μm^2 and more than 80% of it is occupied by the analogue part. The floor plan of the chip is determined by the layout of front-end channels which have to match the layout of multielectrode array outputs (Fig. 4.2). The single front-end channel is 100 μm wide and 3500 μm long. The chip has been designed using full-custom techniques and using the layout rules for a good matching, with a special attention to minimise the effect of the switching noise, as described in section 2.2 and section 3.8.

4.7. Summary of NEURO64 parameters

The developed circuit offers significant flexibility to control the gain and the band over wide ranges. For the applications of this circuit to the measurements of signals from neuronal systems two other parameters are important, namely the total equivalent input

noise and the tolerance to the input offset, which put contradictory requirements on the design concerning the gain of the input stage. If one optimises the circuit for a very low noise performance where the equivalent input noise is about 2 μV rms, the tolerance to the input offset is limited to (–5.5 mV, +4.3 mV), while widening this range to (–13.2 mV, +24.3 mV) the equivalent input noise increases up to 10 μV rms (see section 4.3.2). Due to the fact that the noise performance is limited by the 1/f noise, the requirement concerning the gain of the input stage for which the noise contribution from the following stages is negligible is much higher than in the case when the noise performance is limited by the white noise only.

The essential parameters of the NEURO64 IC for typical bias conditions are summarised in Table 4.3. It is possible to control gain of the circuit from 100 V/V to 10 000 V/V and the cut-off frequencies: the lower one can be tuned from 10 Hz to 130 Hz and the higher one from 400 Hz to 2.8 kHz.

Table 4.3
Summary of basic parameters and test results of NEURO64 chip

Parameter	Measured value
Bandwidth	30 to 1400 Hz
Total equivalent input noise	3 μV rms
Input signal linear range	960 μV_{pp}
Tolerance to the input offset	–8 mV, +11 mV
Gain	1000 V/V
Input signal common mode range	+/–300 mV
Power dissipation per channel	1.7 mW
Power supplies	–2.5 V, +2.5 V
Single channel area	100 μm × 3500 μm

The NEURO64 IC comprises 64 identical channels with all bias and control currents common for all 64 channels. Therefore, the matching of the basic parameters, as gain and cut-off frequencies, is equally important as the parameters themselves. Typical distributions of these parameters measured for one NEURO64 IC are shown in Figure 4.22. The spread of the gain sd./mean = 1.53% is a little higher than obtained from the Monte Carlo analysis. The channels are split into two groups (Fig. 4.22a), which are correlated with the positions of channels on the layout of IC. A similar situation is for the higher cut-off frequency, where two groups of the channels can be seen (Fig. 4.22c). Channels on the right side of the chip (Fig. 4.21) have higher gain and cut-off frequency, than the ones on the left side. The spread of the higher cut-off frequency sd./mean = 1.6% is two times higher than from the simulation. Because the distribution of power supply and control signals is symmetrical across the whole chip, the possible reason of such a situation can be a gradient of the technological parameters such as oxide thickness, threshold adjust implant dose etc. across the wafer. In the performed Monte Carlo simulations (section 4.5), we have not taken into account the variations of V_{T0} and β with the spacing (see equations (4.17), (4.18) and compare with (2.22), (2.27)). We could not see the gradient effects across the wafer in the simulation results.

The measurement of the lower cut-off frequency (Fig. 4.22c) shows an acceptable spread of this parameter sd./mean = 2% which is much smaller than obtained from the simulations (see chapter 4.5) and it is comparable with the measured spread of higher cut-off frequency. That means that probably mismatch parameter of V_{T0} for transistors M28 and M29 (Fig. 4.13), which is given by technology specification and used during the simulations, is overestimated.

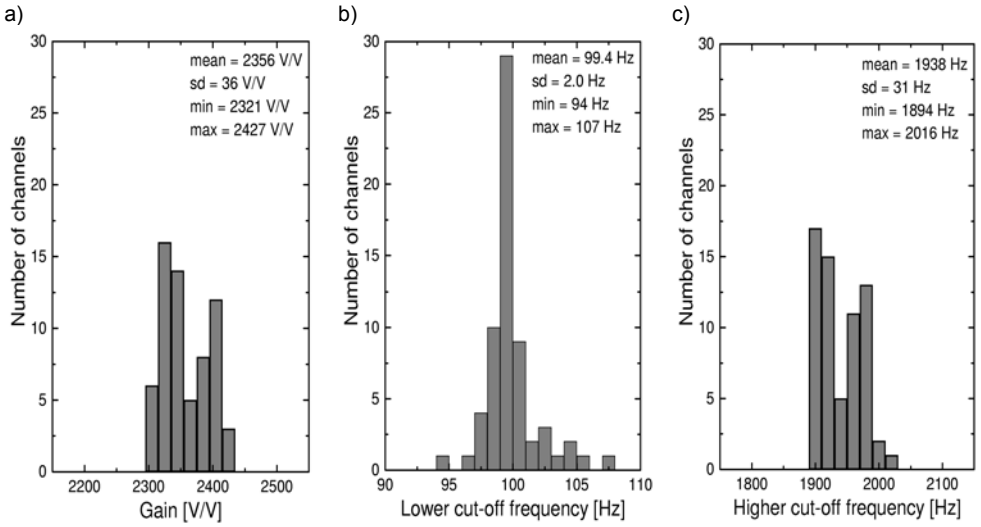

Fig. 4.22. Distribution of analogue parameters in 64 channels of one NEURO64 IC: a) gain; b) lower cut-off frequency; c) higher cut-off frequency

4.8. Neurobiological measurements using NEURO64

Using the multichannel readout system one can measure the response properties of the retinal output neurones, including all spatial and temporal correlations to understand how the retina processes and encodes a visual image. Also the mechanism of retina adaptation can be studied, i.e. dynamic adjustment of sensitivity in retinal neurones that allows visual functioning over a wide range of lighting conditions.

The experimental set-up is shown schematically in Figure 4.23. A live retinal tissue is extracted from the eye of an animal and placed on a planar electrode array inside a cylindrical chamber. The electrodes are arranged in a hexagonal pattern with a row-to-row spacing of 60 μm. The chamber is filled with oxygenated physiological saline solution to keep the retina alive for several hours. A dynamic image pattern, displayed on a computer monitor under the control of the data acquisition system is focused by the microscope onto the photoreceptors. The spikes generated by the output neurones in response to the input pattern are picked by the planar electrodes. The NEURO64 chip amplifies, filters and multiplexes the neuronal signals. From the chip the data are sent and stored on the PC computer. Examples of spikes recorded with the macaque retina are shown in Figure 4.24.

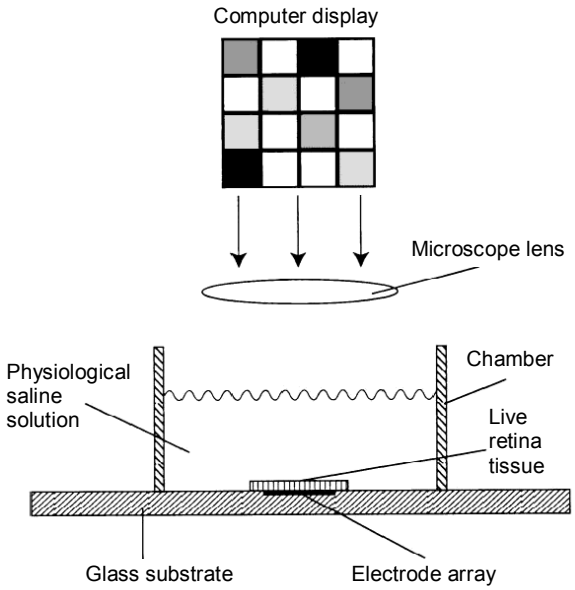

Fig. 4.23. The experimental set-up with the retina readout array to study how the output cells in live retina tissue respond to an image pattern focused on the retina photoreceptors

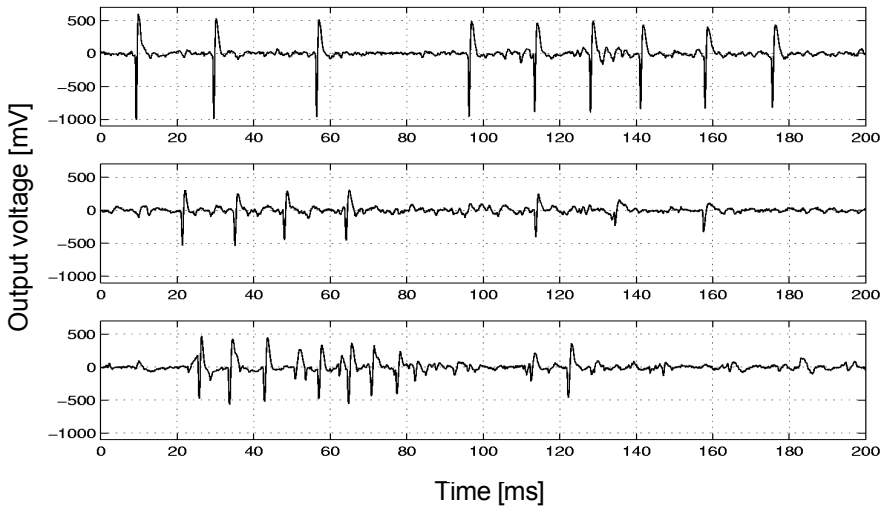

Fig. 4.24. Examples of the signals from macaque retinal tissue recorded with NEURO64